Nanoelectronics from the bottom up

Electronics obtained through the bottom-up approach of molecular-level control of material composition and structure may lead to devices and fabrication strategies not possible with top-down methods. This review presents a brief summary of bottom-up and hybrid bottom-up/top-down strategies for nanoelectronics with an emphasis on memories based on the crossbar motif. First, we will discuss representative electromechanical and resistance-change memory devices based on carbon nanotube and core–shell nanowire structures, respectively. These device structures show robust switching, promising performance metrics and the potential for terabit-scale density. Second, we will review architectures being developed for circuit-level integration, hybrid crossbar/CMOS circuits and array-based systems, including experimental demonstrations of key concepts such lithography-independent, chemically coded stochastic demultipluxers. Finally, bottom-up fabrication approaches, including the opportunity for assembly of three-dimensional, vertically integrated multifunctional circuits, will be critically discussed.

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Over the past four decades, sustained advances in integrated circuit technologies for memory and processors have given us computers with ever more powerful processing capabilities and consumer electronics with ever increasing non-volatile memory capacity[1]. But as device features are pushed towards the deep sub-100-nm regime, the conventional scaling methods of the semiconductor industry face increasing technological and fundamental challenges[1–3]. For example, device size fluctuations may result in a large spread in device characteristics at the nanoscale, affecting key parameters such as the threshold voltage and on/off currents. The increasing costs associated with lithography equipment and operating facilities needed for traditional manufacturing might also create an economic barrier to continued increases in the capabilities of conventional processor and memory chips[1–3].

To continue the remarkably successful scaling of conventional complementary metal oxide semiconductor (CMOS) technology and possibly produce new paradigms for logic and memory, many researchers have been investigating devices based on nanostructures, and in particular carbon nanotubes (CNTs) and semiconductor nanowires[4,5]. For these nanostructures, at least one critical device dimension — the nanoscale wire diameter — is defined during the growth or chemical synthesis process and can be controlled with near-atomic-scale precision. This control, which goes beyond that achievable in top-down lithography, represents one of several key features motivating these efforts. More generally, predictable and well-controlled nanostructure growth implies that materials with distinct chemical composition, structure, size and morphology can be assembled by design to build specific functional devices and integrated circuits[4,5]. This 'bottom-up' paradigm, analogous to the way that biology so successfully works, may prove to be a solution to the technological challenges faced by the semiconductor industry, and could open up new strategies for increasing overall device density by allowing aggressive scaling in three dimensions. Here we review unique features and opportunities of the bottom-up approach to nanoelectronics, assess where it might merge with today's top-down industry, and look at the challenges that must be met to take this area of science towards commercial applications.

NANOSCALE MEMORY ARCHITECTURE

An attractive architecture for using the strengths of the CNT and nanowire building blocks for memory and logic consists of an array of crossed wires[6–8] — the 'crossbar' — as shown in Fig. 1. The assembly of distinct nanoscale wire elements into a crossbar enables the size and function of key device features to be defined during the synthesis of the building blocks and their subsequent assembly, instead of during lithography and processing steps. Specifically, the bit size in the crossbar structure is defined by the diameters of the orthogonal nanoscale wires, the electronic characteristics of the functional element are defined by the two crossed wires (for example, coaxial core–shell materials), and the device density is governed by the density at which the CNTs and nanowires are assembled. This architecture is also attractive owing to its simplicity and the fact that scalable bottom-up techniques have already yielded 2D meshes of chemically synthesized nanowires[9–11], CNTs[12] and molecular devices[13,14].

The crossbar structure can be used for non-volatile memory applications when assembled nanowires yield a configurable junction

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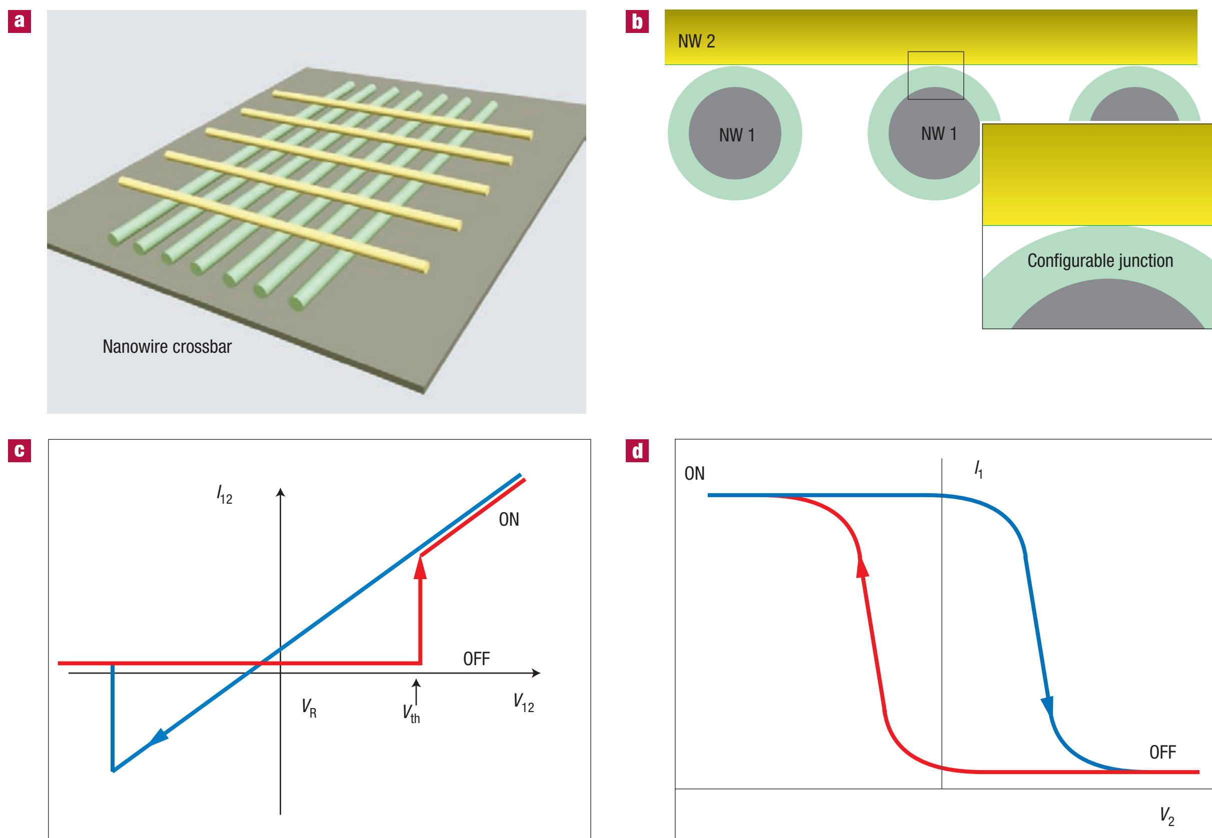

Figure 1 Crossbar memory switches. **a**, Schematic illustration of a nanowire crossbar memory. **b**, Cross-sectional view of the crossbar memory in **a** along a row-nanowire. A memory bit is represented by a configurable bistable junction formed between a pair of column- and row-wires. **c**, Schematic current–voltage (*I*–*V*) curve of a configurable junction that can be modelled as a two-terminal hysteretic resistor. Current I_{12} (voltage V_{12}) is measured (applied) across the column- and row-nanowire pair sandwiching the configurable junction. **d**, In a FET-based crossbar hysteresis is observed in the FET current (I_1) as the voltage on the control wire (V_2) is changed.

at each crosspoint (Fig. 1b). Two general cases can be pictured in which each crosspoint serves as either a resistive switching element (Fig. 1c) or a configurable field-effect transistor (FET; Fig. 1d). In the former case, each crosspoint can be configured independently into a low-impedance ('closed') state or a high-impedance ('open') state simply by controlling the applied voltage between the pair of nanowire electrodes, forming the basis of a memory bit (Fig. 1c). In the latter, each crosspoint FET is configured by the control nanowire which can switch the charge or polarization state of the junction (Fig. 1d). The specific natures of the materials used for the two nanoscale wires in the crossbar and the junction thus define the nature of the memory elements. This conceptual framework has been used for studies of crossbar memory structures based on crossed CNT electromechanical devices[12], bistable molecules[14] and nanowires[15] as discussed below.

The crossbar architecture can in principle be scaled to a memory density level of terabits per square centimetre by reducing the nanowire or CNT average pitch to 10 nm, a feat possible with advanced nanofabrication techniques[16–19] or more simply based on direct assembly[12] of the nanoscale-diameter wires themselves. Dense nanoscale memories, like their CMOS counterparts, will require logic components to write and access stored information. For example, a demultiplexer is a logic component providing address selection and interfacing the high-density memory array with external circuitry. Demultiplexers can be built into the crossbar structure with the same geometry using either nanowire transistors[20] or hysteretic resistor-logic[14]. For more general logic operations, hybrid CMOS/crossbar structures may be required[21–23] in which the CMOS circuitry provides the needed voltage gain and peripheral functions such as input/output, coding/decoding and line driving. The cost of a hybrid approach is increased complexity of chip design and chip area overhead. Alternatively, general computing schemes could be based on a crossbar motif in which nanowire crosspoints function as locally gated FETs[8] or simple hysteretic two-terminal resistors[24,25]. In the latter, signal restoration can be achieved by latches programmed inside the crossbar, although at a cost to operation speed. Key architectural issues and opportunities for nanoelectronics are addressed in greater detail below.

MEMORY ELEMENTS

Molecule-based memories have received considerable attention partly because of the logic that a single molecule would represent the high-density limit for memory bits[6]. Negative differential resistance (NDR) and hysteretic resistance switching have been observed in molecule-based devices formed using break junctions[26], nanopores[27], scanning probes[28,29] and crossbar structures[14,30,31]. The mechanism of the observed device behaviour has been attributed to several effects, including charge-transfer-induced conformational change[32–34], electromechanical switching[35], stochastic conformational changes[28] and metal filament formation[29], where the latter is unrelated to the structures or electrical states of the molecules. This controversy

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about the mechanism of molecule device behaviour may be due in part to the challenges associated with probing molecular states in devices and obtaining well-controlled molecule–electrode interfaces. Performance metrics are also less satisfactory in most molecule-based memories in terms of device yield, on/off ratio, switching speed, endurance cycles and retention time than in existing commercial devices or devices based on CNTs and nanowires. A detailed discussion of molecule-based memory devices can be found in ref. 36.

In addition, a closer examination of molecule-based crossbar memories leads to the observation that the device density is limited by the size of the nanowire electrodes rather than that of the molecules, even in the smallest proof-of-concept devices (for example, around 100 molecules are present at each crosspoint for the 33-nm-pitch device in ref. 31). As a result, even though memories based on single molecules represent the ultimate density potential, this advantage may not come into play until single (or few) molecules can be reliably deposited in arrays with sub-10-nm pitch size, and even then the molecules may not be robust enough for workable memories. In the foreseeable future, we believe high-density crossbar memories will first be produced using a more reliable inorganic or solid-state medium, provided that the storage medium can be scaled in a similar way to the smallest electrodes that can be produced.

One of the first successful implementations of this concept[12] — using the nanoscale wires as both electrodes and functional elements in a crossbar architecture — used the suspended CNT motif shown in Fig. 2a. This crossbar consists of a set of parallel CNTs or nanowires on a substrate and a set of perpendicular single-walled nanotubes (SWNTs) suspended on a periodic array of supports. Each crosspoint in this structure corresponds to a device element with a SWNT suspended above a perpendicular nanoscale wire. Bistability was shown to be possible through the interplay of the elastic energy, which produces a potential energy minimum at finite separation (when the upper nanotube is freely suspended), and the attractive van der Waals energy, which creates a second energy minimum when the suspended SWNT is deflected into contact with the lower wire. These two minima correspond to well-defined OFF and ON states, respectively: the separated upper-to-lower nanotube junction resistance will be very high, whereas the contacted junction resistance will be orders of magnitude lower. Devices can be switched between these OFF and ON states by transiently charging the nanotubes to produce attractive or repulsive electrostatic forces. The viability of this concept was first demonstrated[12] in 2000, and more recently has served as the basis for non-volatile memory chips being developed by Nantero[37]. This electromechanical crossbar switch array has the potential to approach an integration level of 10^{12} elements cm^{-2} with an element operation frequency in excess of 100 gigahertz (ref. 12), although such promise remains to be demonstrated.

Very different strategies for non-volatile memory can also be achieved with the crossbar architecture by using different nanowire materials. For example, by growing nanowires with p-type crystalline silicon (c-Si) cores and amorphous silicon (a-Si) shells, we have recently observed hysteretic resistance switching at Si-nanowire/metal-nanowire crosspoints in which a-Si acts as the information storage medium (Y. Dong, G. Yu, W. Lu, M. C. McAlpine & C. M. Lieber, manuscript in preparation; Fig. 3). Amorphous Si has been extensively studied in the past for potential non-volatile memory applications in planar metal-to-metal (M2M) structures[38,39], where resistance switching was attributed to metal filament formation (retraction) inside the a-Si matrix to yield high (low) conductance ON (OFF) states[39] (Fig. 3a inset). Devices based on M/a-Si/c-Si nanowires have several attractive features that go beyond earlier planar M2M devices. First, they show intrinsic rectification: the device in the ON state behaves like a diode (Fig. 3a), which is desirable for crossbar-based circuits as it mitigates cross-talk between elements[40,41]. Indeed, the bits

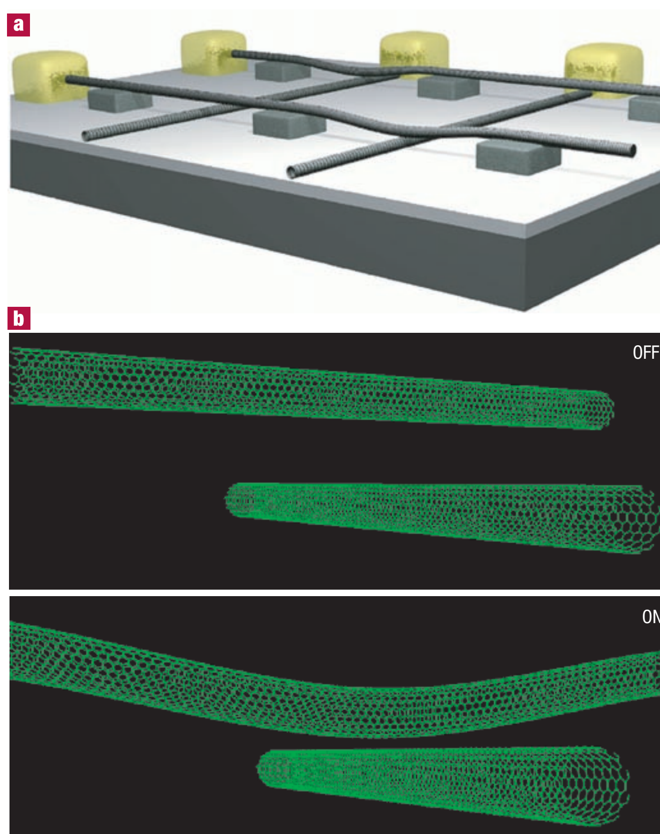

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Figure 2 Electromechanical crossbar memory based on carbon nanotubes. **a**, Three-dimensional view of a suspended crossbar array showing four junctions with two elements in the ON (contact) state and two elements in the OFF (separated) state. The substrate consists of a conducting layer (for example highly doped silicon, dark grey) that terminates in a thin dielectric layer (for example SiO_2, light grey). The lower nanotubes are supported directly on the dielectric film, whereas the upper nanotubes are suspended by periodic inorganic or organic supports (grey blocks). Each nanotube is contacted by a metal electrode (yellow blocks). **b**, Calculated structures of the 20-nm pitch (10, 10) SWNT device element in the OFF (top) and ON (bottom) states. Reprinted with permission from ref. 12.

in multi-element one-dimensional and crossbar arrays (Fig. 3b) can be written, read and rewritten in a fully independent manner (Fig. 3c).

In addition, this a-Si/c-Si nanowire system offers scaling potential comparable to the use of molecules as the storage medium in crossbar memories. We have observed reliable resistance switching and near-100% yield in M/a-Si/c-Si nanowire devices with active device sizes down to 20 nm × 20 nm (limited by the size of the nanowire and lithography resolution), corresponding to a potential device density better than 6×10^{10} bits cm^{-2}, and substantially better than expected from previous work on planar M2M devices where micrometre-sized metal filaments precluded aggressive scaling[39,42,43]. The crossed Si–nanowire/metal–nanowire memory elements show other features that suggest substantial promise as an emerging memory technology. For example, the ON/OFF ratio is typically larger than 10^4 (in comparison, molecular[14,30,31] and chalcogenide[44] elements show ratios under 10^2). The programming current, ~0.01 mA, is much less than that reported for phase-change memories[44], 0.1–0.2 mA, and is more compatible with the minimal MOS transistor drive current desired for high-density integration, whereas the programming speed, <100 ns, is attractive for flash-memory types of applications. These attractive

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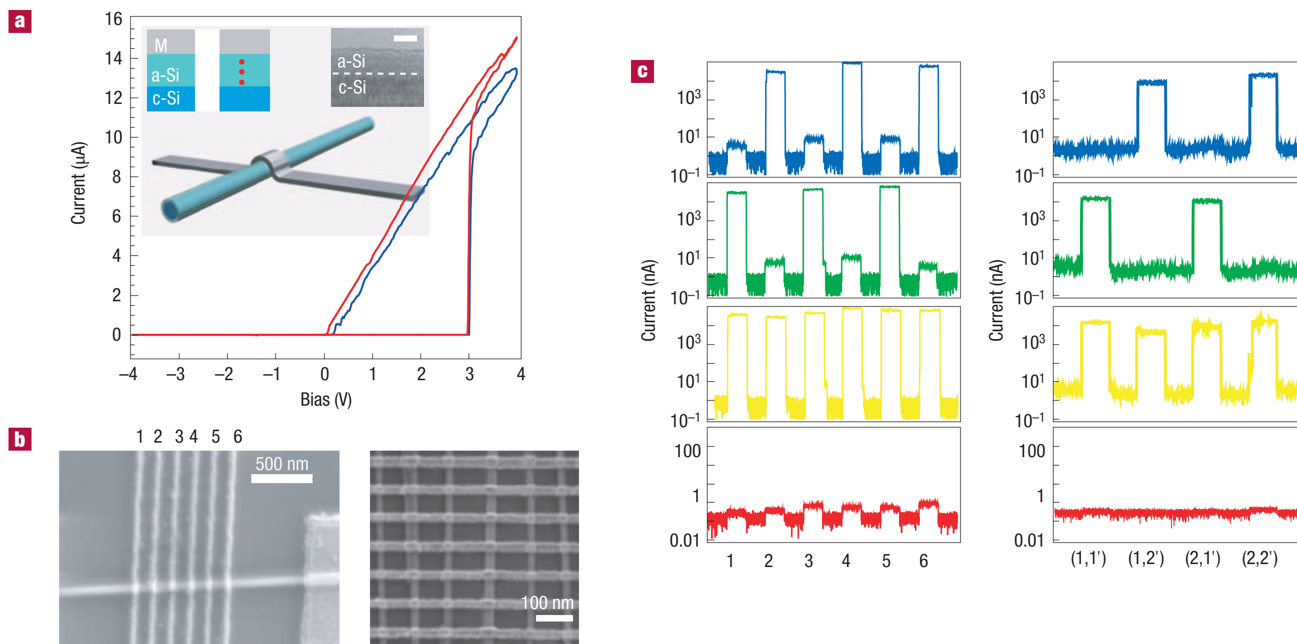

Figure 3 Hysteretic-resistor memories based on core–shell nanowires. **a**, Hysteretic resistance-switching observed at a crosspoint. Unlike the linear schematic curve shown in Fig. 1c, an asymmetric diode-like behaviour can be observed in the ON state. The initial cycle is shown in red and subsequent cycles are in blue. Main inset: schematic of the crossbar memory formed by metal wires (rows) and core–shell nanowires made of a-Si/c-Si (columns). Top left: schematic of a single memory bit showing metal and c-Si electrodes sandwiching an a-Si layer serving as the switchable medium. Top centre: formation of a metal filament inside the a-Si layer changes the memory bit from the high-resistance OFF state to the low-resistance ON state. Top right: high-resolution transmission electron microscope image of a c-Si/a-Si core–shell nanowire. Dashed line indicates the interface between the c-Si and a-Si. Scale bar, 5 nm. **b**, Left panel: scanning electron microscope (SEM) image of a 1 × 6 crossbar array fabricated on a single nanowire with 30-nm metal line width and 150-nm spacing. Right panel: SEM image of a high-density 2D crossbar memory with 100-nm pitch. The core–shell nanowires (columns) were assembled using the Langmuir–Blodgett method and the metal wires (rows) were fabricated using lithography. **c**, Memory bits that can be controllably written and read from the 1 × 6 array and a representative 2 × 2 array. Adapted from Y. Dong, G.Yu, W.Lu, M. C. McAlpine and C. M. Lieber, manuscript in preparation.

characteristics highlight the potential for such bottom-up crossbar arrays, and also suggest that further effort focused on optimizing the endurance and retention time would be worthwhile. Furthermore, the fact that the switching phenomenon is very robust in the nanowire system suggests that high-density memory devices based on the same mechanism may be obtained using commercial top-down fabrication techniques in an all-silicon-based approach. This observation highlights a key point for research in nanoelectronics: besides the ultimate device in which all components are assembled bottom-up at the molecular level, nanostructures may lead to new devices that can in turn result in suitable top-down fabrication for near-term large-scale applications.

The bottom-up approach may also lead to improved performance of memory devices based on conventional structures, or serve as a well-controlled platform for studying the memory mechanism. One such example is crystalline nanowire-based phase-change memory (PCM). PCM has sparked considerable recent interest as a potential next-generation non-volatile solid-state memory technology, and has already been shown to possess many of the necessary attributes, including high resistance contrast, the potential for multilevel storage, and better endurance and write speeds than flash memory. Detailed discussions on PCM can be found in ref. 45. In the bottom-up approach to PCM devices, crystalline nanowires serve as the channel material and can yield reduced PCM reset currents[46–49]. In a PCM, a large current is typically required to heat the channel material enough to yield the amorphous high-resistance reset state. Reduction of the reset current will result in faster amorphization with less power consumption, and allow faster memory switching speed and higher reliability. The reset current is normally lowered by reducing the sample size, which leads to smaller heat capacity per unit length so the device can be heated to sufficiently high temperature with lower joule power[50]. By using GeTe or $Ge_2Sb_2Te_5$ nanowires, it has now been shown[46–49] that currents can be lowered to about 0.4 mA. The reset current could be further reduced by decreasing nanowire diameter, thus confirming the role of channel size in PCM devices suggested by studies on lithographically defined samples[50].

ELECTRONIC CIRCUITS

Recent development of controlled high-yield assembly of crossed nanowire p–n diodes and FETs has enabled the bottom-up approach to be used for assembly of nanoelectronic circuits[10], such as logic gates, that ultimately must be integrated together with memory arrays for read/write operations or to build stand-alone processors. For example, a two-input two-output AND logic gate was assembled from 1(p-Si) × 3(n-GaN) multiple junction arrays (Fig. 4a). The V_o–$V_{i1(i2)}$ data shows constant low V_o when the other input $V_{i2(i1)}$ is low, and nearly linear behaviour when the other input is set at high. Correspondingly, logic-0 is observed from this device when either one or both of the inputs are low, as $V_i = 0$ corresponds to a forward-biased, low-resistance p–n diode that pulls down the output. The logic-1 state is observed only when both inputs are high, as this condition corresponds to reverse-biased p–n diodes with resistances much larger than the constant resistor; that is, little voltage drop across the constant resistor and a high voltage at the output.

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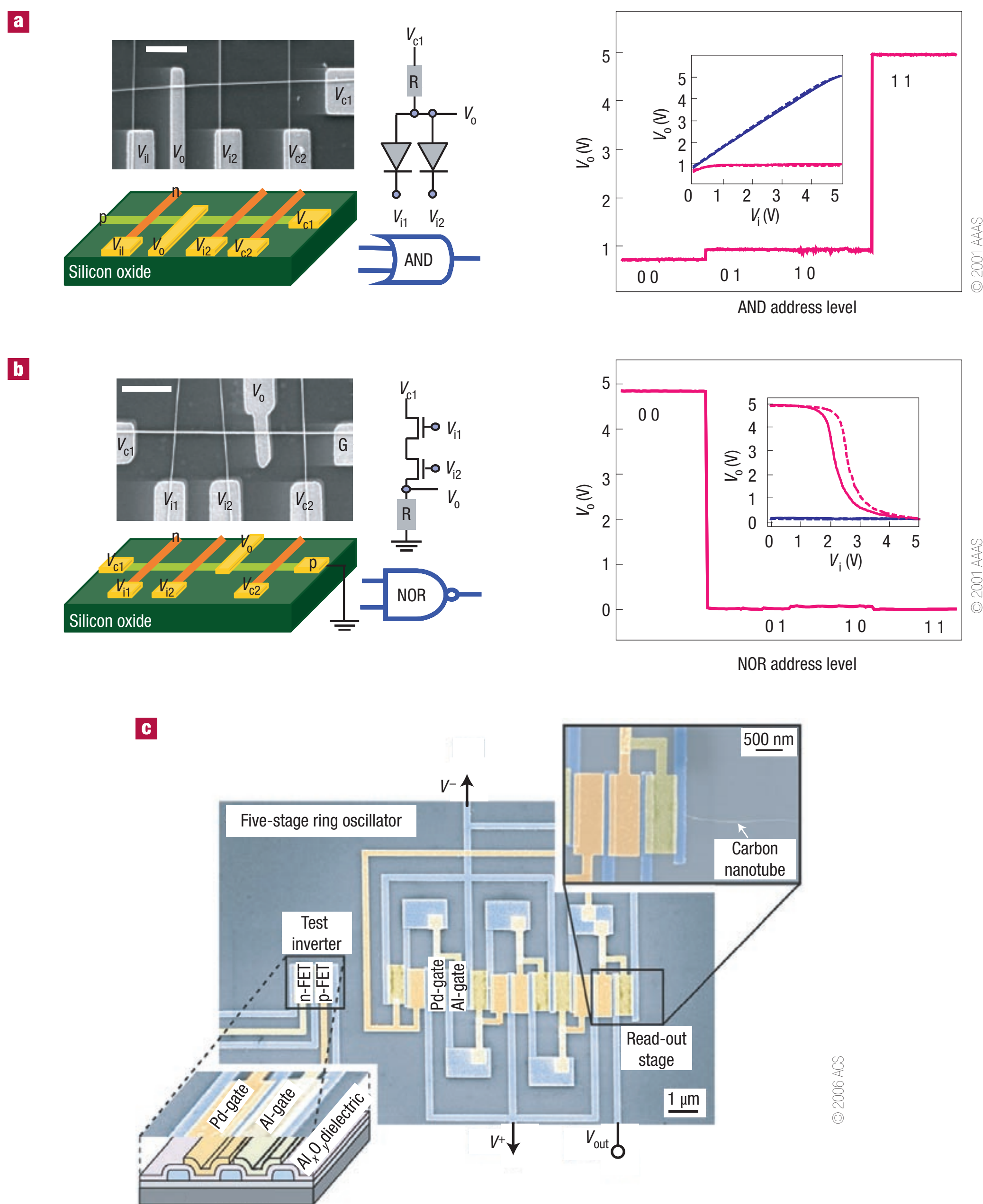

Figure 4 Nanowire and nanotube-based transistor logic. **a**, Left panel: schematic of logic AND gate constructed from a 1 × 3 crossed nanowire array. Insets: a typical SEM (scale bar, 1 μm) of the assembled AND gate and symbolic electronic circuit. Right panel: the output voltage (V_o) versus the four possible logic address level inputs from (V_{i1}, V_{i2}) at preset control (V_{c1}, V_{c2})). Inset: the input and output voltage characteristics, V_o–V_i, where the solid and dashed red (blue) lines correspond to V_o–V_{i1} and V_o–V_{i2} when the other input is 0 (1). **b**, Left panel: schematic of logic NOR gate constructed from a 1 × 3 crossed nanowire array. Insets: an example SEM (scale bar, 1 μm) and symbolic electronic circuit. Right panel: the output voltage versus the four possible logic address level inputs. Inset: the V_o–V_i relation, where the solid and dashed red (blue) lines correspond to V_o–V_{i1} and V_o–V_{i2} when the other input is 0 (1). The slope of the data shows that the device voltage gain is larger than 5. Parts **a** and **b** reprinted with permission from ref. 10. **c**, SEM image of a SWNT ring oscillator consisting of five CMOS inverter stages. Adapted with permission from ref. 51.

In addition, multi-input FET-based NOR logic gates have been studied using assembled 1(p-Si) × 3(n-GaN) crossed nanowire-FET arrays (Fig. 4b)[10]. The V_o–V_i relation of a two-input device shows constant low V_o when the other input is high, and a nonlinear response with large change in V_o when the other input is set low. The logic-0 state is observed when either one or both of the inputs are high. A logic-1 state can only be achieved when both of the transistors are on; that is, both inputs low. Analysis of the V_o–V_i data demonstrates that these two-input NOR gates routinely have gains over five, which is a critical characteristic as it allows interconnection of arrays of logic gates without signal restoration at each stage.

More recently, hybrid bottom-up/top-down approaches have also been used to build circuits based on CNTs and nanowires, including relatively high-frequency oscillators. For example, Avouris and co-workers[51] have demonstrated a CMOS-type ring oscillator on a single long CNT that was assembled on a substrate surface. A key feature

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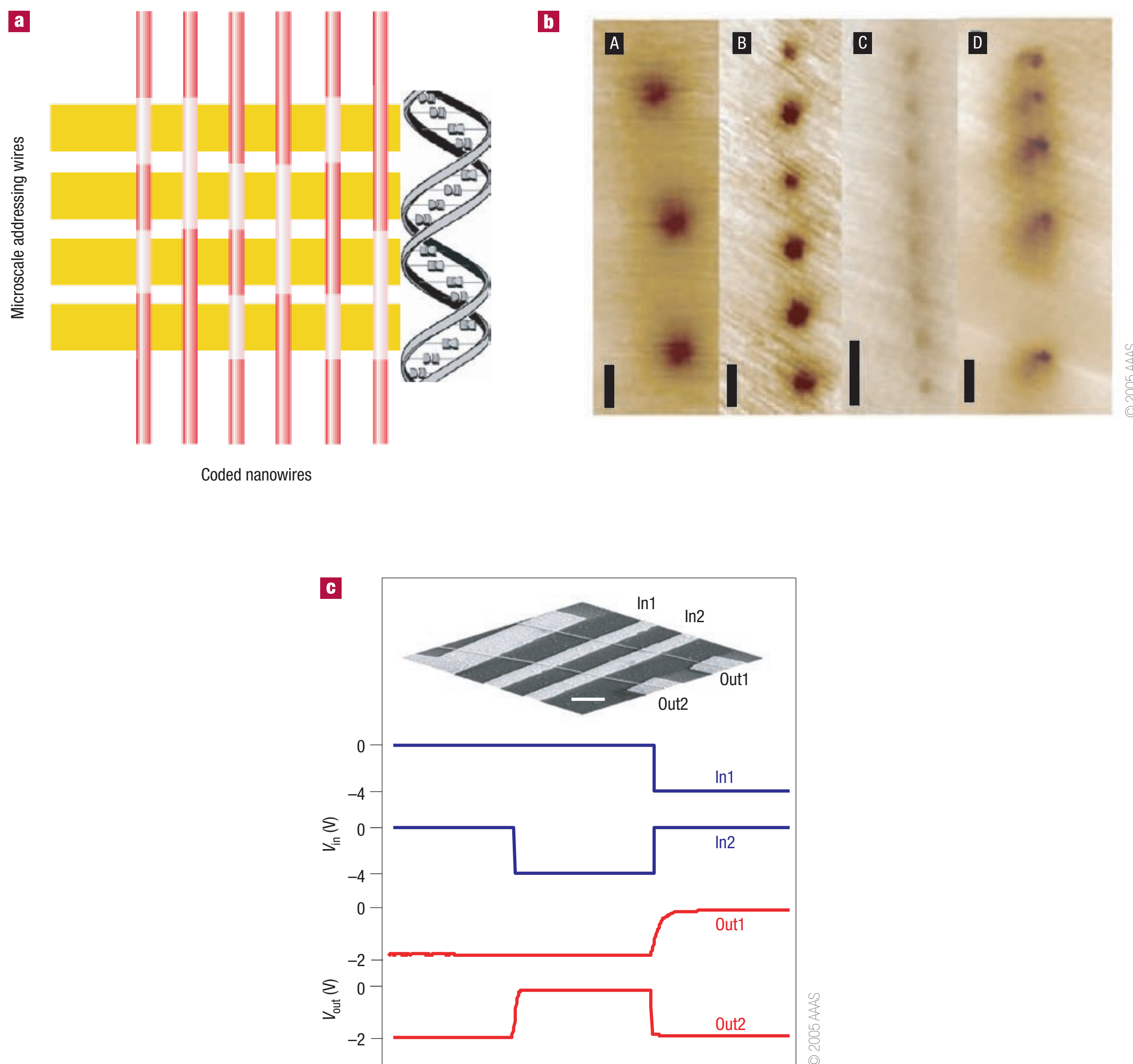

Figure 5 Mixed-scale crossbar demuxes. **a**, Schematic illustration of the mixed-scale demux. Address coding in the nanowires is achieved through modulation doping in a way analogous to gene coding in DNA molecules. The DNA and modulation are not shown to scale. **b**, Scalable synthesis of modulation-doped nanowires with a doping profile of $n^+ - (n - n^+)_N$ for (A) $N = 3$, (B) $N = 6$, (C) $N = 8$ and (D) $N = 5$. Here $n^+(n)$ means heavily (lightly) doped segments and N is the number of repeat units. The results were obtained using a scanning-gate microscopy technique with the lightly doped n-segments shown as the black regions. Both the spacing and length of the doped segments can be controlled during nanowire growth. Scale bars, 1 μm. **c**, Top: SEM image of a 2 × 2 mixed-scale demux configured using two modulation-doped silicon nanowires as outputs (Out1 and Out2) and two gold metal gates as inputs (In1 and In2). Scale bar, 1 μm. Bottom: plots of input (blue) and output (red) voltages for the 2 × 2 demux. Parts **b** and **c** reprinted with permission from ref. 54.

of this work is that it combines the unique electronic properties of single-walled CNTs with controlled top-down lithography to pattern different work-function metals on the CNT so that both n-type and p-type regions can be realized as required for a CMOS device (Fig. 4c). Notably, in this five-stage device, which consists of five p-type and five n-type FETs, signal analysis showed resonances at up to 52 MHz that are consistent with stable oscillation of the device. This combination of strategies could be particularly advantageous for near-term nanoelectronic development, although ultimately hybrid approaches face many of the same constraints that limit conventional top-down processing used in industry today. Furthermore, the one-dimensional nature of nanowires and nanotubes indicates that circuits are more easily built along the long axis of a single nanoscale wire. This offers both design advantages and challenges: on the one hand, the nanowire or nanotube naturally serves as local interconnects and eliminates additional wiring; on the other hand, the success of these devices depends critically on the development of new architectures, including crossbar-motif logic architectures to take full advantage of the unparalleled material and structural control offered by the bottom-up approach.

ADDRESSING NANOARRAYS

Addressing large numbers of memory bits inside a crossbar array will require demultiplexers (demuxes) that allow a relatively small number of control wires to access the large number of nanoscale

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wires selectively inside the memory array. In an ideal demux, n pairs of microscale control wires can be used to select 2^n nanowires; that is, 10 pairs of control wires can specifically address each of the $2^{10} = 1{,}024$ nanowires serving as the columns (or rows) of a 1 Mbit crossbar memory. By using a pair of demuxes serving respectively as row and column selectors, all 2^{2n} crosspoints (memory bits) inside the memory array can be selectively addressed by $2n$ pairs of control wires.

The first prototype crossbar demux was based on the transistor function of semiconductor nanowires[20] in which control wires serve as gate electrodes that cross nanowires extending into and forming the columns or rows of the memory array. 'Address coding' of the nanowires inside the demux was obtained by surface modification during the 'programming' process at specific crosspoints to give them a lower threshold voltage V_T than the unmodified ones[15,20]. The coded nanowire demux effectively forms a NOR plane: the nanowire will be turned off if any one of the control wires crossing it at the modified positions is in the high-voltage '1' state.

Coding specific crosspoints through lithography, however, presents a significant manufacturing challenge for large demux arrays and limits the ultimate scaling advantage of assembled nanowire and CNT building blocks. An intriguing approach that overcomes this lithography barrier involves stochastic demuxes formed using modulation-doped semiconductor nanowires. Threshold voltage modulation and hence address coding is obtained at the different crosspoints between gate wires and the nanowire channel, which may be either heavily or lightly doped (Fig. 5a)[52]. In this approach, the manufacturing cost of lithography and functionalizing specific crosspoints to obtain address coding is exchanged for that of creating modulation-doped nanowires during growth; that is, information is encoded during nanowire synthesis, not by lithography during circuit fabrication. Interestingly, this concept of coding during nanowire synthesis has many analogies with biology where the information is encoded during the synthesis of the linear sequence of bases in a replicated DNA molecule (Fig. 5a).

The stochastic demux scheme is particularly suitable for crossbars based on chemically grown nanowires, because the position registry is generally lost during the assembly using flow-alignment[53] or Langmuir–Blodgett[11] techniques, resulting in arrays of aligned albeit randomly positioned nanowires. Stochastic demultiplexing based on coded nanowires was recently demonstrated by Yang *et al.*[54], where modulation doping along the nanowire axis was achieved with full control of the size, spacing and number of the modulated regions during the growth process (Fig. 5b). Crossed nanowire/microscale control wire demux arrays formed by randomly positioned coded-nanowires were shown to follow predictions[52,54] (Fig. 5c), and thus demonstrate that it is possible to construct a unique demux that is independent of the constraints of lithography used in conventional top-down systems.

In electromechanical and resistive-switching crossbar memories, the memory bits are formed by hysteresis resistors or diodes[14]. By permanently setting specific crosspoints in these resistor arrays to the 'closed' state during the configuration process, wired-OR and AND logic (although with a reduced voltage margin) can be obtained by control wires crossing the same nanowire at the closed points. Using the wired-OR and AND logic, row and column demuxes may be built using mixed-scale crossbars consisting of nanowires leading to the memory array and microscale control wires from the CMOS circuitry. The crosspoints in the mixed-scale crossbar demuxes need to be configured 'permanently' at manufacturing time or during configuration, and should not be affected by the write/erase operations of the memory array. This may require deposition of a different switching medium at the demuxes that shows larger switching threshold voltages compared with inside the memory array. Furthermore, linear resistor logic suffers from limited voltage margin: the voltage difference between the selected and non-selected nanowires may not be large enough to complete the specific write/erase function. To improve the voltage margin, several techniques have been proposed using CMOS coding to eliminate the worst-case scenarios[41,55]. However, considering the limited geometry and functions available in the crossbar resistor-logic, it is reasonable to expect workable demuxes to be in the form of hybrid resistor-crossbar/transistor structures in which the transistor circuitry provides the more difficult functions such as signal gain, restoration, inversion and impedance matching.

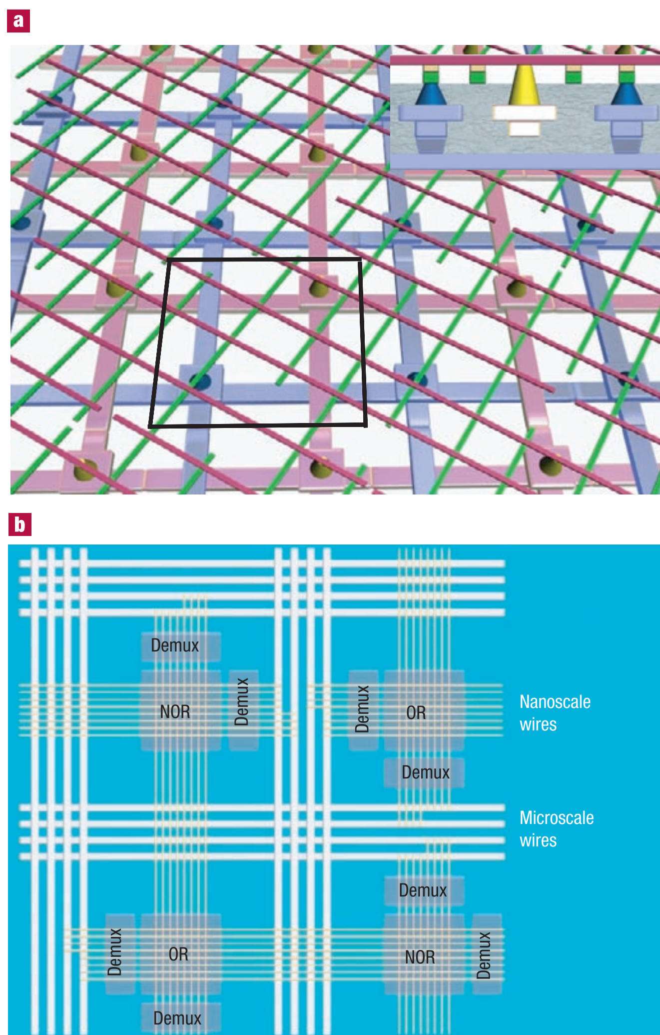

Figure 6 Hybrid crossbar circuits. **a**, Hybrid crossbar/CMOS system based on the CMOL approach. Two sets of pins with different heights separately connect the row and column nanowires in the crossbar with the CMOS circuitry underneath. **b**, Schematic of the array-based system architecture. Each node in the array is a crossbar-based memory or logic device with its own address demux.

HYBRID TO NANO ARCHITECTURES

A hybrid crossbar/CMOS circuit takes advantage of both worlds: the ultra-high device density offered by the crossbar structure and the flexibility offered by the CMOS circuitry. But tradeoffs have to be made: larger crossbar proportion results in higher device density with greater circuit design and fabrication challenges, whereas larger CMOS proportion results in increased circuit functionality at a cost of increased chip area overhead. One hybrid crossbar/

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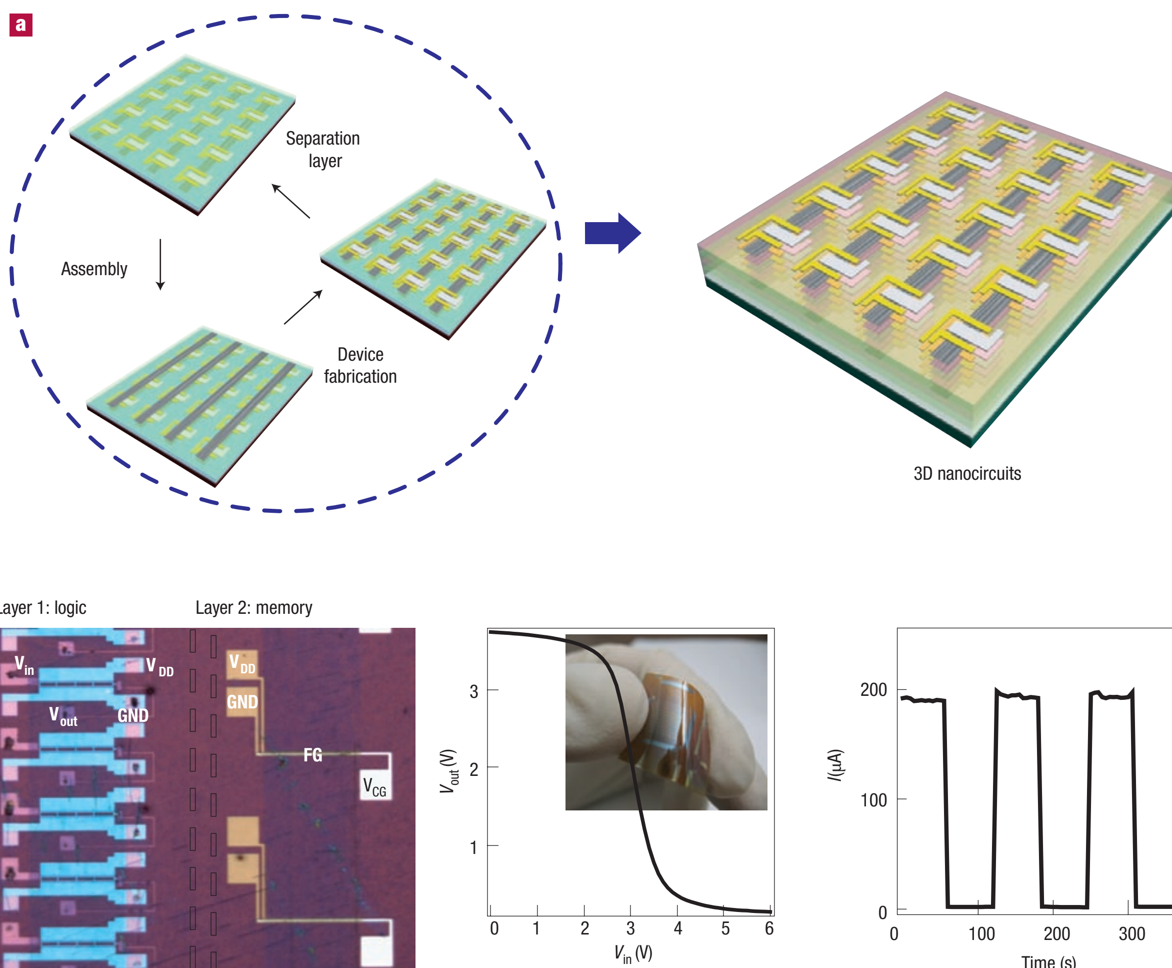

Figure 7 Assembly and integration. **a**, Schematic of three-dimensional integration of multifunctional devices through a layer-by-layer process. **b**, Optical image (left) of nanowire-inverters (layer 1) and floating gate memory (layer 2) on Kapton substrate; d.c. characteristics of the nanowire inverter (centre); switching characteristics of the nanowire floating-gate memory (right). Inset to the centre panel shows functional devices on flexible Kapton substrate. V_{CG}, V_{FG} and V_{DD} are the control gate, floating gate and supply voltages respectively. Reprinted with permission from ref. 59.

CMOS approach that has received considerable attention is the CMOS/nanowire/molecular hybrid (known as CMOL) structure[21,22].

In the CMOL circuit (Fig. 6a), the CMOS-to-nanowire interface is provided by distributing two sets of via-pins uniformly over the whole circuit area. The two sets of pins have different heights so that the taller (shorter) set is connected to the top (bottom) nanowire electrodes in the crossbar array from the CMOS cells underneath. By rotating the crossbar at a small angle (determined by the relative pitch size of the crossbar and CMOS) with respect to the CMOS layer, each nanowire in the crossbar array can be connected to exactly one CMOS cell. In this approach, the most difficult functions — inversion, gain and demultiplexing — are moved into the CMOS layer, using the nanowires solely for data storage (in the case of memories), or wired-OR logic (in the case of logic circuits) and signal routing. A density advantage can still be maintained because only $2n$ CMOS cells are used to control n^2 memory bits; however, the viability of processing on top of a high-performance CMOS structure on which considerable process development/cost has been expended needs to be further scrutinized.

Disregarding practical issues, preliminary studies have shown that CMOL memory with 32-nm CMOS technology could store 1 terabit of data in a 2 cm × 2 cm device[22]. In another hybrid crossbar/CMOS proposal in which even more functions are shifted to CMOS circuitry and the crossbar is used only for data routing[23], easier device fabrication and lower power dissipation are achieved at the cost of lower performance metrics including speed, density and defect-tolerance capabilities. Given these advances, the question seems to have shifted from whether hybrid cross/CMOS circuits are needed to how to implement these structures, and how to optimize the architecture by properly dividing functions between the two classes of components.

Once memory and logic devices (circuits) are implemented, array-based system architectures can be made by interconnecting the crossbar devices such that the output from one crossbar array forms the input of the other (Fig. 6b)[8,21]. The system architecture resembles the nano-architecture at the lower device level: It addresses a similar set of issues such as signal restoration and address demuxing, with the exception that each node in the array is now replaced by a functional memory or logic device. Moreover, the large connectivity of the 2D crossbar arrays provides the possibility to map neuromorphic networks onto distributed crossbar networks in a way that was not possible with CMOS-based approaches, with the potential to achieve artificial neural circuits with comparable density but orders-of-magnitude faster communication speed compared with the cerebral cortex[56].

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DEVICE ASSEMBLY TECHNIQUES

To create large-scale crossbar memory and logic devices from a bottom-up approach, effective assembly techniques are required. Using fluidic assisted alignment, Duan *et al.*[15] and Huang *et al.*[10] have demonstrated prototype crossbar circuits based on crossed nanowire devices. Further progress has also been made on larger hierarchically patterned arrays of aligned and crossed nanowires at centimetre scales[11,57]. In one study[57], a monolayer of aligned nanowires with controlled spacing was first produced through the Langmuir–Blodgett approach, followed by the formation of crossed-wire structures by depositing a second aligned layer at right angles to the first. Photolithography was then used to define a pattern over the entire substrate surface, setting the array dimensions and array pitch. Finally, nanowires outside the patterned areas were removed and metal interconnects could be deposited by conventional lithography.

New assembly methods are still needed for use on a wafer scale where bottom-up and top-down approaches might feasibly be merged, for example, to produce hybrid memory chips. On the other hand, the simple parallel wire structures make the crossbar-based devices suitable for certain top-down techniques, particularly imprint lithography, which offers the potential for high throughput and low-cost fabrication of metal nanowires[16,17,58]. A related approach termed superlattice nanowire pattern transfer (SNAP)[18] uses selective etching of a superlattice edge and subsequent metal deposition to transfer extremely dense parallel arrays of metal nanowires. Using the SNAP technique, a 160-kilobit crossbar memory structure has been demonstrated with silicon (made by selective etching) and titanium wire arrays as the bottom and top electrodes, and a monolayer of bistable rotaxane molecules as the storage medium[31]. The pitch size of the crossbar array was 33 nm, corresponding to a density of 10^{11} bits cm^{-2}, more than 30 times as high as that of the state-of-the-art DRAM or flash devices[1].

Despite these advances the ultimate potential of the bottom-up approach will not be reached unless material-independent assembly methodologies can be developed. One promising approach involves a new dry deposition strategy that enables oriented and patterned assembly of nanowires with controlled density and alignment on substrates from silicon to plastics[59]. The overall process involves optimized growth of designed nanowire material and patterned transfer of nanowires directly from a growth substrate to a second device substrate by means of contact printing (Fig. 7a). Key features include the ability to print aligned nanowires on a wafer scale and to control the density of aligned nanowires through the transfer process. Moreover, this method is readily adaptable to 3D structures. Specifically, repeating the transfer process has enabled up to ten layers of active nanowire field-effect devices to be assembled, and also a bilayer structure consisting of logic in layer 1 and non-volatile memory in layer 2 (ref. 59). This type of capability, and the ability to assemble distinct types of materials almost at will, offers one of the strongest arguments for using the bottom-up approach in the future.

FUTURE PROSPECTS

The ever-growing demand for new nanoscale memories has led to great progress in disciplines including materials growth, assembly/fabrication techniques and new circuit paradigms. It is reasonable to expect bottom-up structures to make their debut in commercial applications as memory devices (which have less stringent requirements) instead of logic devices, although only as effective large-scale and high-throughput assembly processes become available.

In the meantime, many scientific challenges need to be addressed, and we will gain from a critical examination of the diverse approaches mentioned here. For example, can molecules in the nanoscale crossbar memories be replaced by a more reliable solid-state-based switching medium that can maintain the density advantage but offer better performance metrics? Our initial studies on nanoscale resistive switching devices using a-Si as the switching medium seem to affirm this approach.

It is also likely that the next-generation non-CMOS memory device will still have substantial CMOS components — built by hybrid bottom-up/top-down structures at the physical device level, and operated with crossbar/CMOS structures at the architecture level. For example, a memory chip might be composed of imprinted nanoscale metallic crossbars, solid-state switching medium and CMOS logic circuitry that provide addressing, inversion and gain. The daunting task of producing these devices will only be overcome through collaboration between chemists, physicists and electrical and computer engineers.

Further into the future, we expect the bottom-up approach to open many unique approaches for nanoelectronics. Such areas include the development of 3D multifunctional nanoelectronic and hybrid nanoelectronic/biological systems[60] where the capability of assembling CNT and nanowire building blocks in multiple active layers, independent of material or substrate, provides a new way to consider building the future.

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