PRINTED ORGANIC AND MOLECULAR ELECTRONICS

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KLUWER ACADEMIC PUBLISHERS
Boston / Dordrecht / New York / London

Distributors for North, Central and South America:
Kluwer Academic Publishers
101 Philip Drive
Assinippi Park
Norwell, Massachusetts 02061 USA
Telephone (781) 871-6600
Fax (781) 871-6528
E-Mail <kluwer@wkap.com>

Distributors for all other countries:
Kluwer Academic Publishers Group
Post Office Box 322
3300 AH Dordrecht, THE NETHERLANDS
Telephone 31 78 6576 000
Fax 31 78 6576 474
E-Mail <orderdept@wkap.nl>

Electronic Services <http://www.wkap.nl>

Library of Congress Cataloging-in-Publication

Printed Organic and Molecular Electronics
Edited by: Daniel Gamota, Paul Brazis, Krishna Kalyanasundaram, Jie Zhang
ISBN: 1 4020 7707 6

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Printed in the United States of America

4.2 Organic Polymer Field Effect Transistors

Jerzy Kanicki and Sandrine Martin

4.2.1 Introduction

Conjugated organic polymers are a novel class of semiconductors that combine the optical and electronic properties of semiconductors with the advantages of low-cost processing, large-area scalability, compatibility with flexible substrates, and mechanical properties of polymers. Important examples of polymers within this class include poly(p-phenylene vinylene), poly(p-phenylene), polythiophenes, polyfluorene derivatives, and others. In general, the conducting polymers contain extended π-conjugated systems composed of single and double bonds alternating along the polymer chain (for an explanation of π-conjugation, *see* Chapter 2). The strong relation between electronic structure and backbone conformations is a fundamental feature of π-conjugated polymers. The extent of the π-conjugation is the essential structure parameter that controls the physical properties of conducting polymers. Within conducting polymers, carriers can be created by adding impurities. These impurities act as electron donors or acceptors, where the *carrier concentration* depends on the doping level (*i.e.*, amount of impurities present). For example, the introduction of acceptors into a polymer creates holes (positive charge carriers), resulting in structural defects in the alternation of the double and single bonds. These defects can travel along the polymer chain without changing its shape and represent localized solitary waves; they are responsible for localization of the electron states along the polymer chain. The defects can also be called *polarons* if single-charged and *bipolarons* if double-charged. A polaron is a *quasiparticle* that repulses adjacent electrons while attracting the nuclei of neighboring atoms. This results in the polarization of the lattice in its closest vicinity. This accompanying cloud of polarization causes an increased effective mass of the particle, decreasing the mobility of those quasiparticles. Those quasiparticles can be identified by additional energy levels, which appear within the semiconductor bandgap. Polarons in conjugated systems affect not merely the polarization in their vicinity but they can also change the nature of bonds from σ to π and vice versa via excitation and while traveling. The strong electron-lattice coupling is responsible for the existence of polarons in conjugated systems.[1]

In general, the conductivity in polymers is one-dimensional on the molecular scale. Therefore, the polymers can be represented as a one-dimensional disordered system, in which electron states are localized due to defects along the chain. The physical reason for localization is interference of forward- and backward-scattered electron wave functions, forming

standing waves. The situation changes if electrons can be transferred between the chains. If the electrons can move off the chain before they scatter backwards, they become effectively delocalized. Let the inter-chain exchange rate be I_{RE} and the mean free time of an electron moving along chain τ. Then the condition of delocalization is expressed by

$$I_{RE} > \frac{1}{2}\tau \qquad (4.2.1)$$

There exists a threshold value of I_{RE}

$$I_{RE}^{C} \approx \frac{1}{\tau} \qquad (4.2.2)$$

above which electron states become three-dimensional, and below which they are localized on a single chain. Therefore, three-dimensional conductivity will occur when the interchain transfer rate is high enough.[2] However, even if the conductivity in polymers is one-dimensional on the molecular scale, the bulk samples (and device structures) have a three-dimensional conductivity because macromolecules are assembled into three-dimensional structures, and their conductivity will be highly dependent on the thin film morphology. In conducting polymers, one can distinguish *intra-chain* and *inter-chain* transport mechanisms. Intra-chain transport depends on intrinsic properties of macromolecules and the doping level. Inter-chain transport is a function of the polymer morphology and the packing density.

Bulk electronic conduction that is observed in device structures described in this chapter is a result of these processes. If the polymer chain packing is not perfect, inter-chain disorder will reduce the inter-chain transfer rate, and hence decrease the conductivity. It can be argued that polymer chains are packed into a bundle and are well ordered within the bundle, and that the electronic behavior of particular films is controlled by the dimensions and ordering of the bundles. The conductivity in randomly oriented polymers used in OFETs depends on the pathways that are available for carriers to organize a macroscopic electronic current between two contacts. It is expected that the structural order (that can be influenced by solvent polarity, solid content in the solution, thermal treatment and film deposition method) in an intrinsically conducting polymer will have a pronounced influence on its charge transport and device electrical characteristics. For instance, it is expected that the inter-chain transport will

be favorable for high-density crystalline packing of macromolecules because of the relatively small value of the energetic barriers. Therefore, film conductivity will increase with the thermal annealing of samples, leading to an increase in the degree of crystallinity.

In summary, order is one of the key properties of conducting polymers that can have a major effect on electrical performance of devices such as field-effect transistors. The organic materials used in device structures described in this chapter are as-deposited disordered organic polymers.

4.2.2 Device Structures

Since in most of the published papers, the electrical properties of organic thin-film transistors (OFETs) are analyzed using models and carrier transport equations developed for inorganic thin-film transistors (TFTs),[3,4] it is important first to summarize the physics of the TFTs before describing the electrical properties of OFETs. Inorganic TFT operation is based on the crystalline silicon (c-Si) metal-oxide-semiconductor field-effect transistor.

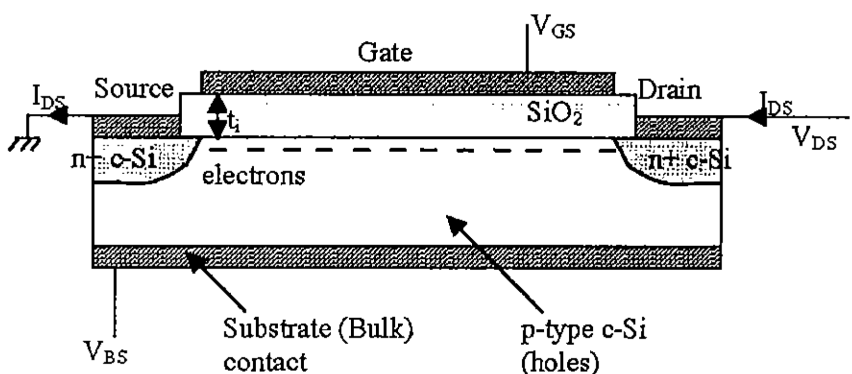

Figure 4.2.1. Typical MOSFET device structure.

The structure of a typical metal-oxide-semiconductor field-effect transistor (MOSFET) is shown in Figure 4.2.1. This cross-section shows an *n*-channel enhancement mode inorganic device built on a *p*-type single crystal silicon (c-Si) substrate, designated as *B* (bulk). The source and drain electrodes are heavily doped *n*-type ($n+$) c-Si regions covered with metal. (An *n*-type material contains impurities, such as phosphorous, which create a

material containing an excess of electrons. Increasing the concentration of dopants generally increases the electrical conductivity of the material.) The heavily doped region creates improved electrical contact between the source and drain electrodes and the metal interconnects used to connect the device to other circuit elements. The gate electrode is separated from the *p*-type c-Si by a gate insulator film (SiO_2) formed by thermal oxidation of the c-Si surface. (A *p*-type material is similar to an *n*-type material, except the dopants create a material with an excess of holes, which are essentially "missing" electrons. Since this missing electron behaves like a positively charged particle, for convenience it is usually treated as such.) Thermal oxidation is a process where a material is heated to a very high temperature (800 to 1200 °C), while being subjected to an oxidizing substance (such as oxygen gas or water vapor). The MOSFET is characterized by its channel length (L), which is the gap between the electrically conductive source and drain electrodes, its channel width (W) (the length of this gap), and the thickness of the gate insulator (t_i). When a positive voltage bias (V_{GS}) is applied to the gate electrode, a conducting channel is formed by accumulation of electrons at the semiconductor/gate insulator interface. This reduces the effective resistance of the path between source (S) and drain (D), allowing the MOSFET drain current (I_{DS}) to flow between the source and drain electrodes if there is a source-drain bias (V_{DS}) applied between them. To collect electrons at the source and drain contacts, *n*+ c-Si regions are needed. The MOSFET is usually a symmetric device in which there is no difference between source and drain; for an *n*-channel device in which the channel carriers are electrons, the source is usually grounded and the substrate-channel junction must be reverse-biased for normal device operation (Figure 4.2.1). This device operates in inversion mode, *e.g.*, electrons are accumulated within a *p*-type semiconductor. Polarities are reversed for a *p*-channel device in which the majority carriers are holes, the substrate is *n*-type c-Si and the source/drain regions are heavily doped *p*-type c-Si (*p*+ c-Si). More details about MOSFETs can be found in Reference 5.

The structure of a typical *n*-channel inorganic thin-film transistor (TFT) is shown in Figure 4.2.2. Many other TFT structures are possible and have been discussed by the authors in Reference 6. In most inorganic TFTs, the active layer is often either hydrogenated amorphous silicon (a-Si:H) or polycrystalline silicon (poly-Si) and is typically 50 to 150 nm thick. Amorphous silicon has virtually no crystal structure, where silicon atoms are randomly arranged. Polycrystalline silicon represents a state between amorphous and crystalline silicon, where some short-range order is present in small crystals that are randomly oriented throughout the material. Since these devices are not fabricated using the more highly-ordered crystalline silicon, both a-Si:H and poly-Si contain defects that introduce electronic

states (trap states) within the semiconductor bandgap. In other words, the defects in the disordered structure create electrical impediments to the flow of electrons and holes. In a-Si:H, these defects are distributed uniformly within the bulk of the film, while in poly-Si they are mostly localized at grain boundaries. In both cases, the Fermi level in the undoped material is typically near midgap level. The Fermi level is a mathematical indicator of the type and concentration of overall doping (natural or due to added impurities) in a material. When it is at midgap, essentially an equal number of electrons and holes are present in the material. A material in an "undoped" state is referred to as an "intrinsic" material. Therefore, doping of a-Si:H and poly-Si is possible and both *n*- and *p*-type materials can be produced. When *n*-type material is used for the channel material, the source and drain contacts use heavily doped *n*-type (*n*+) a-Si:H regions while *p*+ a-Si:H source and drain contacts are used for *p*-channel TFTs. This device arrangement is the opposite of what is used in MOSFETs. The gate insulator of most TFTs is amorphous silicon oxide (a-SiO_x:H, essentially glass) or amorphous silicon nitride (a-SiN_x:H, a common insulating material in microelectronics) deposited by plasma-enhanced chemical vapor deposition (PECVD). PECVD is a deposition process that uses radio-frequency (RF) discharge and gas mixtures. The excited species flow over the substrate and form a thin film on the top of the substrate. In *n*-channel TFTs, electrons accumulate near the gate insulator/semiconductor interface when a positive voltage bias is applied on the gate electrode, see Figure 4.2.2. In TFTs, there is no creation of an inversion layer but rather an accumulation layer, composed of majority carriers, is formed at the semiconductor/gate insulator interface. In other words, in an *n*-channel device, the conductive layer at the semiconductor/ gate interface is composed of a large number of electrons; in a *p*-channel device, this layer consists of holes.

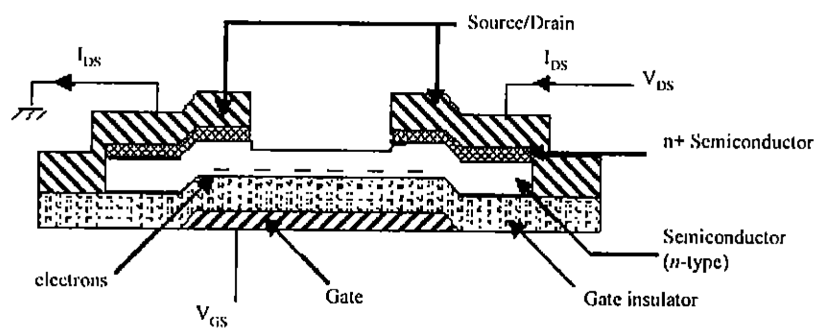

Figure 4.2.2. Typical TFT device structure.

In organic thin-film transistors (OFETs), the semiconductor active layer is a thin organic film (having a thickness t_{SC}), which can be fabricated by vacuum deposition, printing, or from solution (by spin-coating for instance).[7] The OFET structure is often very similar to the one of the inorganic amorphous or polycrystalline semiconductor TFTs, Figure 4.2.3. OFET device structures can be divided into two categories: coplanar and staggered structures. In coplanar OFETs, the gate, source and drain electrodes are all located on the same side of the organic semiconductor film. In staggered devices, the gate electrode is on the opposite side of the organic semiconductor film from the source and drain electrodes. Staggered OFETs are further subdivided into top- or bottom-gate OFETs, depending on the position of the gate electrode, on the top or bottom side of the organic semiconductor film, respectively. Examples of OFET cross-sections are shown in Figure 4.2.3. Independently of the OFET device structures shown in Figure 4.2.3, there are different possible source-drain electrode arrangements. Figure 4.2.4 shows top views of standard, Corbino, and interdigitated device structures. In all these devices, the source and drain electrodes (traditionally often Au or ITO) are usually directly in contact with the organic semiconductor, *i.e.*, without the use of a heavily doped interfacial layer, as it is common in inorganic devices. Like inorganic devices, the OFET is also characterized by the channel length (L) between source and drain electrodes and the channel width (W). The gate insulator can again be composed of traditional microelectronics materials, such as thermal silicon dioxide (SiO_2), amorphous silicon oxide, amorphous silicon nitride, aluminum oxide, or others (see Section 4.2.6.4). Patterned gate electrodes can be made of metals such as chromium, aluminum, or transparent conducting oxides such as indium tin oxide (ITO). When a non-defined gate electrode is used (this is typical practice when new organic semiconducting materials are being evaluated), highly doped (n+) c-Si is often used as the gate electrode and thermal SiO_2 is often used as gate insulator. It should also be noted that most organic semiconductors are naturally p-type, and therefore most OFETs are p-channel devices operating in accumulation enhancement mode. As described before, this means that holes are the majority carriers, which accumulate and create a conductive path at the gate insulator/organic semiconductor interface. Attempts to dope organic semiconductors have often led to ambiguous results. Typically, the preferred route to n-channel devices is to use a naturally n-type material. So far, major problems with n-type organic semiconductors are attributed to material instability with respect to oxygen. However, n-type organic semiconductors for OFETs have recently been produced.[8]

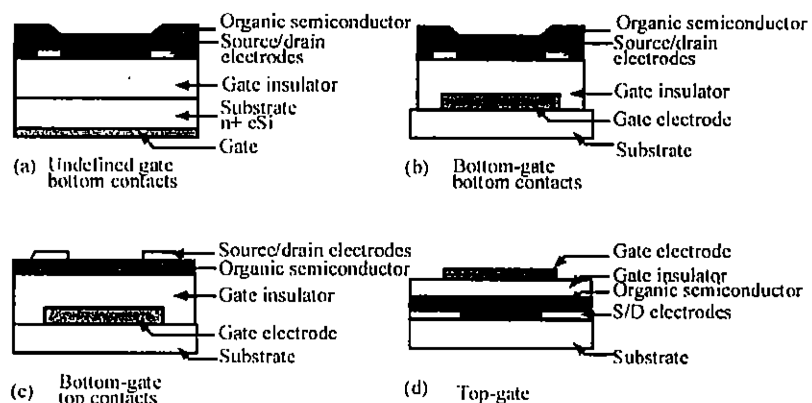

Figure 4.2.3. Examples of OFET device structures. (*a*) Coplanar OFET with non-defined gate electrode. (*b*) Coplanar OFET with defined gate electrode. (*c*) Staggered bottom-gate OFET. (*d*) Staggered top-gate OFET.

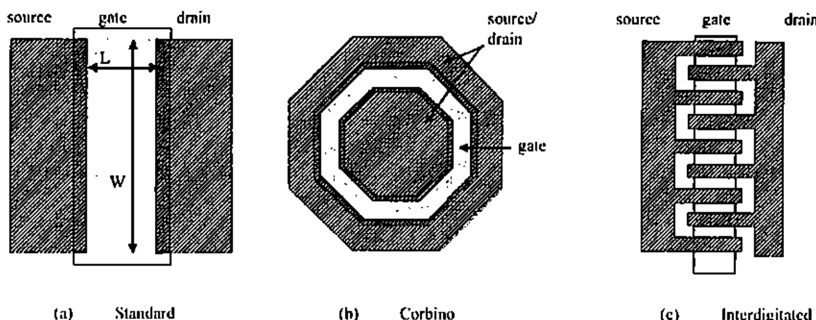

Figure 4.2.4. Top-views of OFET device structures. (*a*) Standard OFET. (*b*) Corbino OFET. (*c*) Interdigitated OFET.

4.2.3 Device Operation Principles

4.2.3.1 c-Si MOSFET Operation

The theory of operation of a MOSFET is well known and will not be discussed in detail here. However, some of the basic principles that are most

useful for OFET analysis will be described. Note that the following section is intended to describe transistor operation in detail in order to give the reader a detailed, quantitative understanding of FET operation. The reader is walked through the derivation of the most important equations used to describe the transistor operation. Full understanding of this material may require at least some background in semiconductor device physics, due to the large amount of terminology and detail in this section. A conceptual description of transistor operation can be found in Section 4.2.2.

For an *n*-channel MOSFET under a positive gate voltage bias (V_{GS}), thermally generated free electrons are capacitively induced (*i.e.*, appear on the opposite end of the gate insulator when a voltage is applied to the gate) at the semiconductor/gate insulator interface. These minority carriers (holes outnumber electrons) create an inversion channel or space charge (in other words, a conductive path) in the *p*-type bulk c-Si, the MOSFET is therefore said to operate in inversion mode. The charge in the semiconductor is composed of the depletion charge, associated with the depletion (*i.e.*, removal) of majority carriers (holes) and the inversion charge, associated with the accumulated electrons at the semiconductor/gate insulator interface (channel). When the concentration of electrons in the channel region becomes higher than the hole concentration in the bulk of the semiconductor, the device is in the strong inversion regime, as shown in Figure 4.2.5.

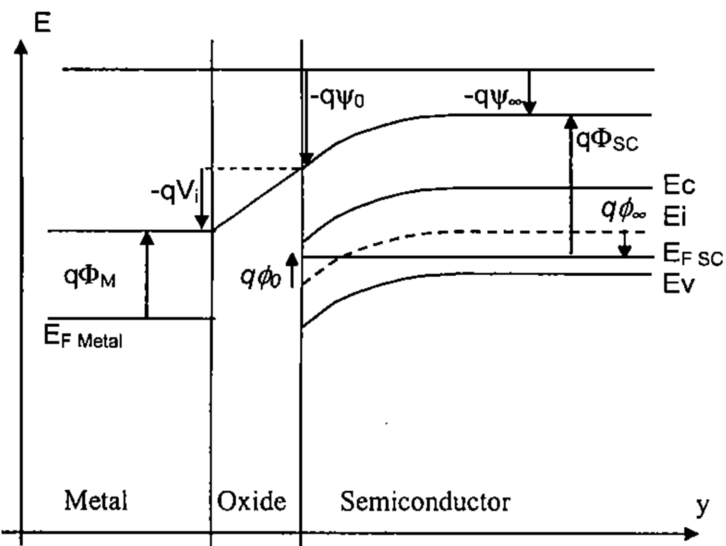

Figure 4.2.5. Typical electronic band structure of an *n*-channel MOSFET in inversion regime.

Here it is assumed that the band bending does not significantly change with further increase of the gate voltage and, based on the balance of charges in the structure, the conduction channel (or inversion) charge can be expressed as

$$Q_{cond} = -C_i(V_G - V_{SC}) + C_i(\Phi_M - \Phi_{SC}) - Q_{depl} - 2C_i\phi_\infty \quad (4.2.3)$$

where Q_{cond} is the conduction charge, C_i is the gate insulator capacitance per unit area, V_G is the voltage applied on the gate, V_{SC} is the voltage applied on the semiconductor, Φ_M is the metal work function, Φ_{SC} is the semiconductor work function, Q_{depl} is the depletion charge and φ_∞ is the potential difference between the Fermi level and the intrinsic level in the bulk of the semiconductor. For a *p*-type semiconductor,

$$\phi_\infty = -\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) < 0 \quad (4.2.4)$$

where N_A is the density of acceptor dopants (*p*-type semiconductor) and n_i is the intrinsic carrier density. If the variations of Q_{depl} with the gate voltage and along the conduction channel are neglected, the resolution of Poisson equation gives

$$Q_{depl} = -\sqrt{-4qN_A\varepsilon_{SC}\varepsilon_0\phi_\infty} \quad (4.2.5)$$

where ε_{SC} is the semiconductor dielectric constant and ε_0 is the vacuum permittivity (also known as the *permittivity of free space*). The device threshold voltage, also supposed to be independent of the gate voltage and the position along the conduction channel, can be defined as

$$V_T = (\Phi_M - \Phi_{SC}) + \frac{\sqrt{-4qN_A\varepsilon_{SC}\varepsilon_0\phi_\infty}}{C_i} - 2\phi_\infty \quad (4.2.6)$$

The expression of the conduction charge then becomes

$$Q_{cond} = -C_i(V_G - V_{SC} - V_T) \quad (4.2.7)$$

If a source-drain voltage is applied between the source and drain electrodes and if it is assumed that the Fermi potential gradient is mostly along the *x*-axis (gradual channel approximation), the current density is, for an *n*-channel device

$$J_n(x) = -q\mu_n n \frac{d\varphi_n}{dx} \tag{4.2.8}$$

where $d\varphi_n/dx$ is the gradient of the Fermi potential in the semiconductor channel. Consequently, the drain current $I_{DS} = I_D = -I_S$ is obtained

$$I_{DS}(x) = -\iint J_n dydz = -\mu_n \frac{d\varphi_n}{dx} WQ_{cond}(x) \tag{4.2.9}$$

where it has been assumed that the current I_{DS} is positive when flowing from drain to source, *i.e.*, in the negative *x*-axis direction. Combining Equations 4.2.7 and 4.2.9, the following equation is obtained

$$I_{DS}(x) = \mu_n WC_i \frac{d\varphi_n}{dx}[(V_G - V_{SC}(x)) - V_T] \tag{4.2.10}$$

Because the current flowing through the channel is constant, the following relationship is made

$$I_{DS} = \frac{1}{L}\int_0^L I_{DS}(x)dx \tag{4.2.11}$$

which results in, assuming that the field-effect mobility, μ_n, does not depend on x

$$I_{DS} = \mu_n \frac{W}{L} C_i \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4.2.12}$$

where μ_n is the field-effect mobility of the electrons, W and L are the channel width and length, respectively, C_i is the gate insulator capacitance per unit area and V_T is the MOSFET threshold voltage as defined by Equation 4.2.6. This model assumes that the source-drain voltage is sufficiently low so that the entire conduction channel (from source to drain) is in strong inversion. It also assumes that the depletion charge and, consequently, the threshold voltage, depend mostly on the gate voltage, and that their dependence on the position in the conduction channel can be neglected. These assumptions correspond to the so-called *MOSFET gradual channel approximation.*

Equation 4.2.12 is valid as long as the whole channel remains in accumulation, *i.e.*, there is no channel pinch off. This assumption is true for

$$V_{DS} \le V_{GS} - V_T \tag{4.2.13}$$

For larger values of the source-drain voltage, the current saturates and is given by

$$I_{DS} = \mu_n \frac{W}{2L} C_i (V_{GS} - V_T)^2 \tag{4.2.14}$$

Ideally, the values of μ_n and V_T used in both equations (linear and saturation regimes) should be the same. However, these two different operation regimes of the MOSFET are not affected equally by second-order effects and this can result in slight discrepancies between the linear and saturation parameters.

Before the MOSFET reaches strong inversion, it is said to be in the subthreshold regime. In this case, the band bending in the semiconductor still depends significantly on the gate voltage. Solving the Poisson equation (*see* Equation 4.2.23) yields the following expression of the conduction channel charge

$$Q_{cond} \approx -kT\sqrt{\frac{N_A \varepsilon_{SC}\varepsilon_0}{2q(\phi_0 - \phi_\infty)}} \cdot e^{\frac{q(\phi_0 + \phi_\infty)}{kT}} \tag{4.2.15}$$

where φ_0 is the potential difference between the Fermi level and the intrinsic level at the semiconductor/gate insulator interface. This equation becomes, after assuming that the device is close to the onset of strong inversion and making a few approximations

$$Q_{cond} \approx -kT\sqrt{\frac{-N_A \varepsilon_{SC}\varepsilon_0}{4q\phi_\infty}} \cdot e^{\frac{q(V_G - V_{SC}(x) - V_T)}{nkT}} \tag{4.2.16}$$

The expression of the MOSFET current is then

$$I_{DS}^{subthreshold} = \mu_n \frac{W}{L} kT \sqrt{\frac{-N_A \varepsilon_{SC}\varepsilon_0}{4q\phi_\infty}} \left(\frac{nkT}{q}\right) e^{\frac{q(V_{GS} - V_T)}{nkT}} \left[1 - e^{-\frac{qV_{DS}}{nkT}}\right] \tag{4.2.17}$$

where an additional parameter has been introduced

$$n = 1 + \frac{1}{2C_i}\sqrt{-\frac{qN_A\varepsilon_{SC}\varepsilon_0}{\phi_\infty}} \qquad (4.2.18)$$

From the MOSFET drain current expression, the subthreshold swing, S, is defined by

$$S = \left(\frac{d \log I_{DS}^{subthreshold}}{dV_{GS}}\right)^{-1} \qquad (4.2.19)$$

which yields

$$S = \frac{nkT}{q\log(e)} = \frac{kT}{q\log(e)}\left(1 + \frac{1}{2C_i}\sqrt{-\frac{qN_A\varepsilon_{SC}\varepsilon_0}{\phi_\infty}}\right) \qquad (4.2.20)$$

Consequently, in an ideal MOSFET, the subthreshold swing is associated with the density of acceptors in the bulk of the semiconductor.

4.2.3.2 Inorganic TFT Operation

Inorganic TFTs operate differently than the c-Si MOSFET. In these TFTs, there is no depletion region and current can flow between source and drain even when there is no bias voltage on the gate electrode. In this case, the level of this source-drain *leakage current* depends on the film thickness and electronic quality, as indicated by the following equation

$$I_{leakage} \approx \frac{\sigma_d dWV_{DS}}{L} \qquad (4.2.21)$$

where σ_d is the semiconductor dark conductivity, and d its thickness. In general, low off-currents can be obtained in TFTs because of the characteristically low electrical conductivity of the inorganic amorphous or polycrystalline semiconductors. Since the TFT operates in accumulation mode, which is different from most MOSFETs, which operate in inversion mode, care has to be taken when using equations derived for MOSFETs to describe the TFT operation.

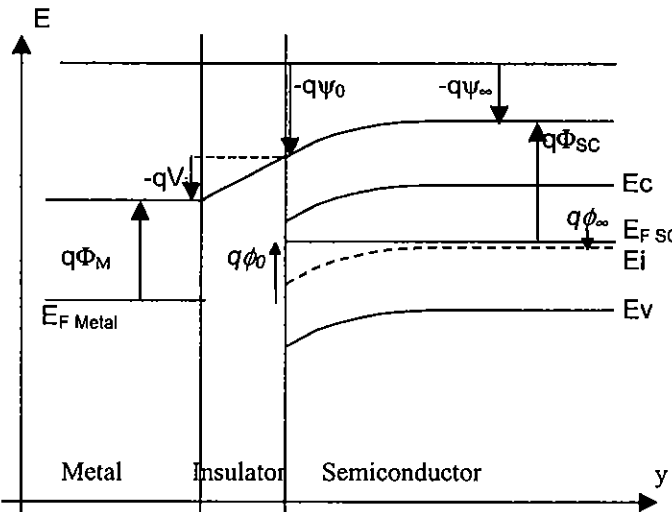

Figure 4.2.6. Typical electronic band structure of an *n*-channel TFT in accumulation regime.

The main difference between the c-Si MOSFET and the a-Si:H TFT is the expression of the charge in the semiconductor, which does not involve a depletion charge (as the semiconductor is usually not doped), but includes contributions from carriers trapped at states present in the inorganic semiconductor bandgap. Figure 4.2.6 shows the electronic band diagram of an *n*-channel TFT in the accumulation regime. The equations describing the TFT operation in the accumulation and subthreshold regimes are established in a similar way to what has been done for the MOSFET, by taking into consideration the balance of charges in the device structure

$$V_G - V_{SC} = (\Phi_M - \Phi_{SC}) - \frac{Q_{SC}}{C_i} + (\phi_0 - \phi_\infty) \qquad (4.2.22)$$

and the Poisson equation

$$\frac{d^2\phi}{dy^2} = -\frac{\rho(y)}{\varepsilon_{SC}\varepsilon_0} \qquad (4.2.23)$$

Often, different non-idealities of the device structure and materials have to be included when establishing the equations above. First, the contributions of the fixed charges within the insulator layer or at the semiconductor/gate insulator interface (Q_i) may have to be included

$$V_G - V_{SC} = (\Phi_M - \Phi_{SC}) - \frac{Q_{SC}}{C_i} + (\phi_0 - \phi_\infty) - \frac{Q_i}{C_i} \qquad (4.2.24)$$

In addition, the density of defect states at the semiconductor/gate insulator interface (N_{ss}) may also need to be considered. Assuming that these density of states distributions are constant within the semiconductor bandgap and that the states are donor-type below midgap and acceptor-type above midgap, their contribution to the device charge is

$$Q_{ss} = -q^2 N_{ss} (\phi_0 - \phi_\infty) \qquad (4.2.25)$$

Finally, defect states (N_T) are also present in the bulk of the semiconductor and need to be taken into account in the balance of charges and for the solution of Poisson equation. Assuming that there is a constant distribution of defect states within the semiconductor bandgap, donor-type below midgap and acceptor-type above midgap, their contributions to the semiconductor density of charge is

$$\rho_T(y) = -q^2 N_T \phi(y) \qquad (4.2.26)$$

Because of the complex expression of these non-idealities, solving Poisson and balance of charge equations is not as simple as for c-Si MOSFETs, even in the accumulation regime.[6,9,10,11] However, after a few approximations, it is usually possible to obtain equations describing the n-channel TFT operation in the accumulation regime, in the linear, and the saturation regime, respectively, that are similar to the ones developed for c-Si MOSFETs

$$I_{DS}^{lin} = \mu_{FE} C_i \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (4.2.27)$$

and

$$I_{DS}^{sat} = \mu_{FE} C_i \frac{W}{2L}(V_{GS} - V_T)^2 \qquad (4.2.28)$$

In this case, the mobility μ_{FE} is the device field-effect mobility, which is usually lower than the free carrier band mobility because of the presence of gap states. The threshold voltage V_T is not directly associated with the characteristics of the materials, as in the case of the c-Si MOSFET (Equation 4.2.6), but is defined by the gate voltage for which the TFT conduction charge equals zero. Charges present in the insulator film or at the gate insulator/ semiconductor interface only result in a voltage shift of the TFT characteristics, *i.e.*, shift of V_T without a change in Equations 4.2.27 and 4.2.28. On the other hand, defect states in the semiconductor or at the gate insulator/semiconductor interface would affect the device characteristics and response. In addition, if defect states having an exponential energy dependence (such as band tails) in the amorphous or polycrystalline semiconductor bulk are taken into account, the expression of the charge localized on the defect states is more complex and the expressions of the TFT current (Equations 4.2.27 and 4.2.28) need to be modified. More details on this subject are provided in References 6-11.

When the TFT is in the weak accumulation regime, the calculation is similar to that used for the MOSFET, but taking into account the contribution of defect states to the semiconductor charge is critical. Assuming that there is a constant density of states N_T in the bulk of the semiconductor and a density of surface states N_{ss} at the semiconductor/gate insulator interface, an expression similar to Equation 4.2.17 can be obtained

$$I_{DS}^{subthreshold} = I_0 \exp\left(\frac{qV_{GS}}{nkT}\right)\left(1 - \exp\left(\frac{qV_{DS}}{nkT}\right)\right) \qquad (4.2.29)$$

with n now defined as follows

$$n = 1 + \frac{\sqrt{q^2 N_T \varepsilon_{SC} \varepsilon_0}}{C_i} + q^2 \frac{N_{ss}}{C_i} \qquad (4.2.30)$$

Using the same definition as for the MOSFET (Equation 4.2.20), the following expression of the subthreshold swing is obtained

$$S = \frac{kT}{q\log(e)}\left[1 + \frac{\sqrt{q^2 N_T \varepsilon_{SC} \varepsilon_0}}{C_i} + q^2 \frac{N_{ss}}{C_i}\right] \qquad (4.2.31)$$

The subthreshold swing S increases with increasing density of defect states. From this equation, is can be concluded that the separation of the

individual contributions of N_T and N_{ss} to S is not possible from the analysis of S alone. Other experimental methods should be used to determinate N_T and N_{ss} independently from each other. For example, electron spin resonance method can be used to measure N_T and capacitance–voltage technique can be used to find N_{ss}.

It is noted that, if the density of defect states in the amorphous semiconductor is constant within the semiconductor bandgap, the *Debye screening length* (L_D) can be defined. It represents the distance over which the electrical field penetrates into the semiconductor film. The Debye screening length is given by the following equation

$$L_D = \sqrt{\frac{\varepsilon_{SC}\varepsilon_0}{q^2 N_T}} \qquad (4.2.32)$$

In general, if the bulk density of defect states N_T is not constant over the gap, the Debye screening length is still expected to be correlated to the distance over which the electrical field penetrates into the semiconductor film. Typical values for inorganic semiconductors are 250 nm for a-Si:H ($N_T \sim 10^{16}$ cm^{-3}·eV^{-1}) and 50 nm for poly-Si ($N_T \sim 3 \times 10^{17}$ cm^{-3}·eV^{-1}). It should be noted that small values of the screening length or a high density of defects would make the semiconductor unattractive for TFT applications. To obtain low TFT OFF-current, the undepleted region of the TFT should be maximized, *i.e.*, a large Debye screening length is desired.

The TFT equations for *p*-channel devices would be very similar to the equations developed above for *n*-channel TFTs, with only a change of sign resulting from the majority carriers being holes instead of the electrons that are present in *n*-channel TFTs.

4.2.3.3 OFET Operation

It is now well established that the physics of the carrier transport is, in many respects, different from that of inorganic thin-film amorphous semiconductors. Nevertheless, OFETs exhibit electrical characteristics that are very similar in many respects to those of thin-film inorganic semiconductors.[12]

An important and general feature of organic polymers is that they are not well-ordered materials, where any crystalline phases present are always made of small, imperfectly ordered crystallites. Hence, the disorder present in organic polymers has an important electronic consequence, which is localization (*i.e.*, trapping) of charge carriers. Furthermore, the conformation of the chain within the microcrystalline polymers has static

fluctuations along its length, with the inter-chain interactions fluctuating as well. The potential fluctuations due to these effects are spread over some distance and usually are not very deep (so-called *weak disorder*). On the other hand, chemical defects, such as non-conjugated carbon atoms inserted within the chain or other impurities, may result in strong local potential variations (so-called *strong disorder*). Both types of disorder are important in limiting the conjugation length and in affecting the carrier transport within OFETs. The effect of disorder in organic polymers and its impact on OFET operation principle is a complicated problem and will not be addressed in this chapter. It is argued that weak disorder may be the main source of localization and the limitation of conjugation length. However, simultaneous trapping of a charge by deep gap states located at well-defined energies can generate a "localized" (*i.e.*, trapped) polaron, which can have a very long lifetime: of seconds or more. Organic polymers seem therefore to be different from amorphous silicon, in which localized state energies form continuous distributions (so called *band tail states*), extending deep into the gap. However, in amorphous inorganic semiconductors, localized deep-gap sates in addition to band tails are present. Generally, traps are expected to yield field-effect mobilities, which are both much lower than microscopic ones and vary with physical or electronic properties of the materials.

In general, organic field-effect transistors exhibit so-called *p*-channel behavior (where the majority carriers are holes) within a *p*-type organic semiconductor. Thus, when the gate electrode is biased positively with respect to the grounded source electrode, the channel region is depleted of carriers. This results in a high channel resistance (which is referred to as the '*off*' *state*). When the gate electrode is biased negatively, OFETs operate in the *accumulation mode*. In this state, a large concentration of holes is accumulated within the device channel, resulting in a low channel resistance (which is referred to as the '*on*' *state*). The accumulation layer is believed to be limited to the first few monolayers at the organic semiconductor/gate insulator interface. It has been shown that an organic semiconductor layer with a thickness equivalent to only few such monolayers is sufficient for proper OFETs operation, with additional thickness not substantially increasing the device 'on'-current.[8] The magnitudes of these 'on'- and 'off'-currents and the time required to switch between these two states determine the utility of a transistor in a organic circuits. The OFETs must produce enough 'on'-current to activate or switch another part of a circuit, but it must not generate off-currents that are large enough to cause unwanted switching.

To describe the OFET operation, the simplest model can be based on a *p*-channel thin-film transistor as developed for inorganic TFTs. In the accumulation regime, the drain current is given by the following equations, characterizing the linear and the saturation regimes, respectively