# THIN-FILM TRANSISTORS

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# 3

# Hydrogenated Amorphous Silicon Thin-Film Transistors

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## 3.1 MOTIVATION

This chapter focuses on issues related to the engineering of high-performance hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) suitable for large-area high-resolution active-matrix liquid crystal displays (AMLCDs). In particular, the underlying physics, numerical simulation, and characterization of a-Si:H TFTs and a-Si:H advanced TFT structures are described.

Ever since the solid-state revolution, silicon-based devices and integrated circuits have replaced most of the conventional circuitry in electronics. The change is so significant that the lives of almost everyone in the world have been affected. Vacuum tubes, once dominant composing elements of electronic appliances such as computers and radios are now historic exhibits and can hardly be seen without going to a museum. However, vacuum tubes have not completely disappeared from our lives. The giant vacuum cathode ray tubes (CRTs) still remain the major information display terminal for television and computers. Yet

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the CRT is gradually being replaced by the emerging technology of flat-panel displays (FPDs). The advantages of FPDs are obvious, especially for portable applications such as laptop computers, medical imaging X-ray sensors, and avionic displays. Today, it is also clear that the heavy and bulky CRTs will soon become history just like their other vacuum counterparts. In fact, the commerical battle between CRTs and FPDs is very intense. The main reason for FPDs' not having completely taken over the CRT market is that they cost more than CRTs, but the gap is closing every year. In fact, 2003 is expected to be the first year when FPD revenue will exceed that of CRTs.

Among various FPDs, the dominant product on the market is liquid crystal displays (LCDs). There are two types of LCDs: passive and active addressing modes; the advantages of the former lay in its low cost, while the latter enables high-resolution displays. For active-matrix LCDs, silicon (amorphous or polycrystalline) thin-film transistors serve as the key pixel electrode–switching element. Hydrogenated amorphous silicon is well suited for AMLCDs because it can easily be deposited over large areas at low temperatures that are fully compatible with glass or plastic substrates. In addition, it has a high dark resistivity, leading to TFTs with low leakage currents. Films of a-Si:H can be *n*- or *p*-doped to allow for the fabrication of low-resistance contacts. The processing of a-Si:H TFTs is similar to the crystalline silicon metal oxide–semiconductor (MOS) integrated circuit technology, which makes AMLCDs more mature than other technologies, such as organic displays based on light-emitting devices. Finally, a-Si:H technology benefits from the tremendous investment in a-Si:H solar cells made several years ago, and so has become the dominant player in the active-matrix display world.

## 3.2 NUMERICAL SIMULATION OF AMORPHOUS SILICON THIN-FILM TRANSISTORS

Since hydrogenated amorphous silicon thin-film transistors were described by LeComber et al. in 1979 [1], they have been widely used as switching devices in active-matrix liquid crystal displays [2]. To improve the electrical performance of a-Si:H TFT for high-resolution AMLCDs, for instance, it was important to evaluate how the a-Si:H density-of-states (DOS) and the TFT source/drain series resistances affect the device electrical performance [3–5]. It was expected that a good understanding of a-Si:H physics combined with the a-Si:H DOS model would substantially reduce the time and cost of a-Si:H TFT process optimization.

Device modeling can be preliminarily divided into two fields: analytical modeling and numerical modeling. In the early days only analytical modeling could be achieved because of limited computer resources for numerical modeling. The advantage of analytical modeling of a-Si:H TFTs [6–9] is that the device performance and design parameters are related by a closed-form equation, helping

the understanding and improvement of the device electrical performance. Furthermore, analytical modeling can be integrated easily into existing CAD tools such as SPICE for circuit simulation. However, for a device with more complicated materials or structures, it is difficult to derive a closed-form equation that can represent the device physics. For instance, it is more difficult to model a-Si:H TFTs analytically than metal oxide–silicon field-effect transistors (MOSFETs) because the a-Si:H large density-of-states makes it difficult to solve Poisson's equation and other differential equations. Furthermore, analytical modeling has difficulty dealing with two- or higher-dimensional structures. Therefore, analytical modeling often has to simplify the device structure into one dimension. However, some structures, such as the a-Si:H TFT with thin semiconductor layer, cannot be simplified into a one-dimensional structure, and any simplifying assumptions made during the derivation will limit the accuracy of obtained results.

Although it is time consuming and difficult to incorporate into circuit simulators, numerical modeling usually provides a more flexible method in the modeling of devices, so different model assumptions may be analyzed and compared. The numerical method resolves basic semiconductor equations such as Poisson's and continuity equations without any simplifications. Based on these equations, the influence of different distributions of density of states and source/drain contact resistances can be analyzed from the point of view of two-dimensional current flow.

### 3.2.1 Simulation Model

Today the most popular structure for a-Si:H TFTs is the inverted-staggered structure shown in Figure 3.1. The semiconductor layer consists of intrinsic a-Si:H and heavily $P$-doped ($n^+$) a-Si:H. The gate insulator is usually hydrogenated

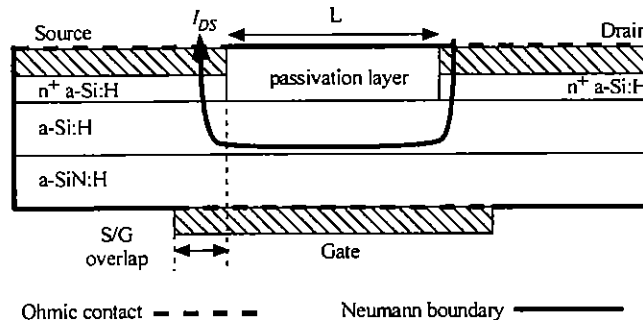


**Figure 3.1** Cross section of the a-Si:H TFT structure used for numerical simulations. (Adapted from Ref. 19 with permission from Elsevier Science.)

amorphous silicon nitride (a-$SiN_x$:H). The inverted-staggered a-Si:H TFT operates in the accumulation mode. When a positive voltage is applied to the gate electrode, the band bending at or near the gate insulator/amorphous semiconductor interface is increased and electrons accumulate near the interface to form the conduction channel. If a positive drain voltage is applied to the drain electrode, the drain–source current flows from the drain to the source electrodes through $n^+$ a-Si:H, intrinsic a-Si:H, and conduction channel (see Fig. 3.1).

If the electrostatic potential and quasi-Fermi levels are known as a function of position, all the physical phenomena can be determined. To calculate these three variables, the two-dimensional Poisson's equation and continuity equations are solved simultaneously [10]. Poisson's equation is given by

$$\nabla\cdot(\varepsilon\nabla\psi) = q[p - n - \sum(N_A^- - N_D^+)] \tag{3.1}$$

where $\varepsilon$ is the permittivity of a-Si:H, $\psi$ is the electrostatic potential, $q$ is the electronic charge, $p$ and $n$ are electron and hole concentrations, respectively, and $N_A^-$ and $N_D^+$ are the concentrations of ionized acceptor-like and donor-like states, respectively.

The continuity equations for electrons and holes, respectively, are as follows:

$$-\frac{1}{q}\nabla\cdot J_n = G_n - R_n \tag{3.2}$$

$$\frac{1}{q}\nabla\cdot J_p = G_p - R_p \tag{3.3}$$

where $J_n$ and $J_p$ are the current density for electrons and holes, respectively, $G_n$ and $G_p$ are the generation rates ($cm^{-3}s^{-1}$) for electrons and holes, respectively, and $R_n$ and $R_p$ are the recombination rates ($cm^{-3}s^{-1}$) for electrons and holes, respectively. The net recombination rate through every defect state is given by the Shockley–Read–Hall formulation [11].

The two-dimensional a-Si:H TFT structure is decomposed into a discrete mesh structure by the finite-element method. Grid points are placed nonuniformly and depend on the estimated distribution of carrier concentrations. The area near the a-Si:H/a-$SiN_x$:H interface and the source/drain-gate overlap have denser grid points. A larger number of grid points can improve the accuracy of simulation but will also increase computation time. To ensure an acceptable compromise, the number of grid points is increased until the simulation results are within 2% of variations: for a 10 μm-channel-length a-Si:H TFT, the total number of grid points in our device structure is about 800. Once the grid points are determined and drain and gate voltages are set, the simulation program resolves the nonlinear partial differential equations (Poisson's equation, electron and hole continuity equations) using Newton's method [10] and $\psi$, $n$, and $p$ as unknowns. All the physical parameters, such as current, electrostatic potential, electron concentra-

tion, hole concentration, electrical field, and energy band bending, can be calculated.

### 3.2.1.1 Boundary Conditions

Two types of boundary conditions are used in this simulation: ohmic contact and Neumann (reflective) boundary. These boundaries are illustrated in Figure 3.1. The contacts between source/drain metal and $n^+$ a-Si:H, and gate metal and gate insulator interfaces are assumed to be ohmic. On the other hand, the outer edges of a-Si:H TFT are assigned to be Neumann boundaries. Ohmic contacts are considered as simple Dirichlet boundaries, where the boundary fixes the electrostatic potential and the electron and hole concentrations along the boundary. For a given specific contact resistance ($R_c$ in $\Omega$-cm$^2$), the electrostatic potential $\psi$ is determined by

$$\psi = \psi_{\text{ref}} + V_a - \frac{R_c}{A} I_a \tag{3.4}$$

where $A$ is the area of the boundary, $\psi_{\text{ref}} = E_c - E_F/q$ at the terminal, $E_F$ is the Fermi-level position, $V_a$ is the terminal voltage, and $I_a$ is the terminal current.

On the other hand, the outer edges of the a-Si:H TFT are assumed to be limited by the Neumann boundary conditions, so the current flows out of the device only through the drain and source contacts. Assuming no surface charges on such edge, the normal components of the electrostatic potential and carrier concentration gradients are set to zero:

$$\frac{\partial \psi}{\partial \hat{r}} = \frac{\partial n}{\partial \hat{r}} = \frac{\partial p}{\partial \hat{r}} = 0 \tag{3.5}$$

where $\hat{r}$ is the direction perpendicular to the external boundary.

Traditionally, the MOSFET boundary conditions are based on the semi-infinite semiconductor assumption; i.e., the width of the space-charge regions (or the effective Debye length) is much smaller than the thickness of the semiconductor, and the band bending decreases to zero in the bulk of the semiconductor layer ($d\psi/dy = 0$ and $\psi = 0$ at $y = t_{\text{a-Si:H}}$) However, these boundary conditions are not always applicable to a-Si:H thin-film transistors [12–14]. Thin a-Si:H layers (500–2500 Å) and low free-carrier density will allow the depletion region to extend over the entire semiconductor layer. Thus the traditional boundary conditions at the interface between the a-Si:H and the passivation layer cannot be applied to a-Si:H TFTs.

The set of the three-coupled nonlinear partial differential Eqs. (3.1), (3.2), and (3.3) are numerically solved for every grid point at given drain, source, and gate biases. Examples of the simulated static transfer characteristic in linear and

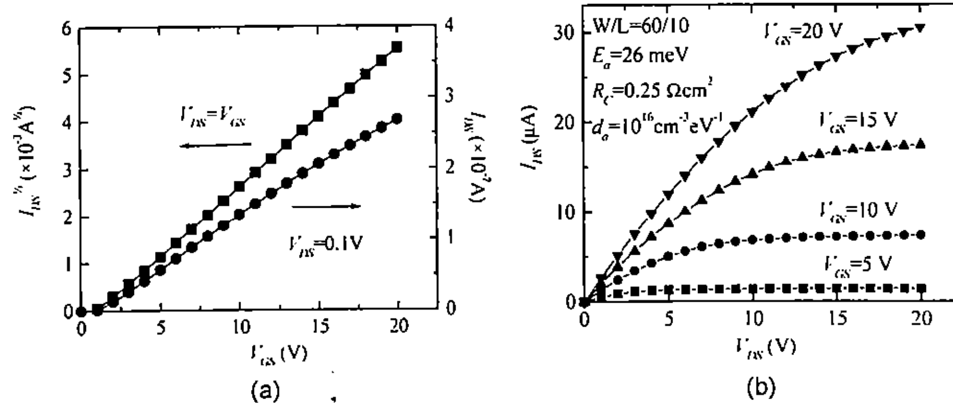


**Figure 3.2** (a) Simulated transfer characteristics in linear and saturation regimes. (b) Simulated output characteristics. (From Ref. 15.)

saturation regimes are shown in Figure 3.2a [15]. The field-effect mobility ($\mu_{FE}$) and threshold voltage ($V_T$) were extracted in linear and saturation regions [16] using the gradual channel approximation equations:

$$I_{DS} = \frac{\mu_{FE} C_i W}{L} (V_{GS} - V_T) V_{DS} \tag{3.6}$$

for $V_{DS} = 0.1$ V (linear region), and

$$I_{DS} = \frac{\mu_{FE} C_i W}{2L} (V_{GS} - V_T)^2 \tag{3.7}$$

for $V_{DS} = V_{GS}$ (saturation region), where $C_i$ is the gate insulator capacitance per unit area, $L$ is the channel length, $W$ is the channel width, $V_{GS}$ is the gate–source voltage, and $V_{DS}$ is the drain–source voltage. An example of output characteristics is shown in Figure 3.2b.

### 3.2.1.2 Amorphous Silicon Density-of-States Model

The model of the density-of-states for a-Si:H proposed by Davis and Mott [17] is adopted in this simulation. The states present in the a-Si:H electronic gap consist of two types: band-tail states and deep-gap states. For numerical simulation, the continuous distributions of both acceptor- and donor-like states within the mobility gap was approximated by several discrete energy states. A total number of

90 discrete energy states with an 0.02 eV interval constitutes a trade-off between accuracy and computation time.

The distributions of band-tail states are given by Eqs. (3.8) and (3.9):

$$g_{CBa} = g_{ta} \exp\left(\frac{E - E_c}{E_a}\right) \tag{3.8}$$

$$g_{VBd} = g_{td} \exp\left(-\frac{E - E_v}{E_d}\right) \tag{3.9}$$

where $g_{ta}$ and $g_{td}$ are the densities of acceptor- and donor-like tail states at $E = E_C$ and $E = E_V$, respectively, and $E_a$ and $E_d$ are the characteristic slopes of the conduction- and valence-band tails, respectively. The valence-band-tail states are below the Fermi level and have negligible influence on a-Si:H TFT electrical characteristics in the ON-state. This is not the case for the conduction-band-tail states, which can significantly affect the a-Si:H TFT electrical performance. Transfer characteristics in the saturation region calculated for different $E_a$ values are shown in Figure 3.3a: the corresponding $\mu_{FE}$ decreases and $V_T$ increases when $E_a$ increases. We should note that the lower $E_a$ values are associated with a-Si:H film having an enhanced short-range order.

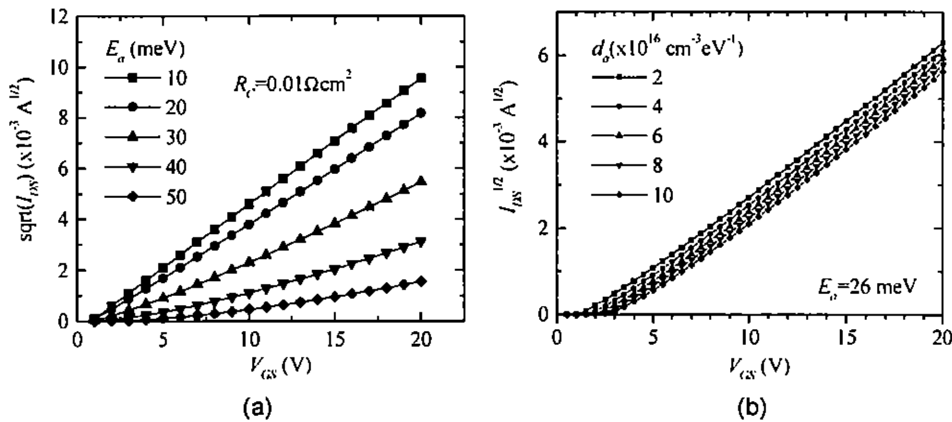


FIGURE 3.3 Simulated transfer characteristics in the saturation regime for (a) different conduction-band-tail slopes and (b) different peak values of deep-gap states. (From Ref. 15.)

The deep-gap states are modeled by two Gaussian-like distributions representing the donor- and acceptor-like traps:

$$g_{DGa} = d_a \exp\left(-\frac{(E - \lambda_a)^2}{\sigma_a^2}\right) \tag{3.10}$$

$$g_{DGd} = d_d \exp\left(-\frac{(E - \lambda_d)^2}{\sigma_d^2}\right) \tag{3.11}$$

where $d_a$ and $d_d$ are the peak values of the Gaussian distribution of acceptor- and donor-like deep-gap states, respectively, $\lambda_a$ and $\lambda_d$ are the mean energies of the Gaussian distributions of acceptor- and donor-like states, respectively, and $\sigma_a$ and $\sigma_d$ are the standard deviations of the Gaussian distributions of acceptor- and donor-like states, respectively. The description and default values for these equations and typical geometry parameters used in this simulation are listed in Table 3.1.

Simulated transfer characteristics are plotted in Figure 3.3b for peak values of deep-gap states, $d_a$ ranging from $2 \times 10^{16}$ to $10^{17}$ $cm^{-3}eV^{-1}$. The TFT field-effect mobility is not affected, but the threshold voltage increases with increasing $d_a$.

### 3.2.1.3 Source and Drain Contact Resistances

Based on the current flow shown in Figure 3.1, the a-Si:H TFT source/drain series resistances consist of three parts: (1) the specific contact resistances between the source/drain metal electrodes and the $n^+$ a-Si:H layers; (2) the resistances of $n^+$ a-Si:H film; and (3) the resistances due to the intrinsic a-Si:H layers between the source/drain $n^+$ a-Si:H layers and the conducting channel (a-Si:H/a-$SiN_x$:H interface). Parts (2) and (3) will be discussed in section 3.3.4.

In general, the contact resistance depends on the specific contact resistance ($R_C$) and the contact area. Today $R_C$ is limited by the poor doping efficiency of $n^+$ a-Si:H, and it is about 0.1–1 $\Omega$-$cm^2$ with current a-Si:H TFT technology. For a given source/drain metallurgy, one way to reduce the contact resistance is to increase the doping efficiency of $n^+$ a-Si:H. Kanicki [18] showed that when the $n^+$ a-Si:H film resistivity ($R_f$) is reduced from 100 to 10 $\Omega$-cm, the $R_C$ decreases from 30 to 0.1 $\Omega$-$cm^2$. The experimental relation between $R_f$ (in $\Omega$-cm) and $R_C$ (in $\Omega$-$cm^2$) for Mo/$n^+$ a-Si:H contacts can be described by [18]

$$\log(R_c) = -1 + 1.25 \log(R_f) \tag{3.12}$$

For large $R_C$, a nonnegligible portion of the applied drain voltage drops on the high source/drain contact resistances, leading to a reduced field-effect mobility [19].

**TABLE 3.1** Parameters Used for the Numerical Simulations, Unless Specified Otherwise

| Parameter | Value | Description |
|---|---|---|
| $\lambda_a$ (eV) | 0.98 | Mean value of Gaussian-distributed acceptor-like deep-gap states |
| $\sigma_a$ (eV) | 0.2 | Variance of the Gaussian-distributed acceptor-like deep-gap states |
| $\lambda_d$ (eV) | 0.56 | Mean value of the Gaussian-distributed donor-like deep-gap states |
| $\sigma_d$ (eV) | 0.17 | Variance of the Gaussian-distributed donor-like deep-gap states |
| $\sigma_n$ ($cm^2$) | $10^{14}$ | Electron capture cross section of the conduction-band-tail states |
| $\mu_{n0}$ ($cm^2/Vs$) | 8 | Electron mobility in conduction-band extended states |
| $\sigma_p$ ($cm^2$) | $10^{14}$ | Hole capture cross section of the valence-band-tail states |
| $\mu_{p0}$ ($cm^2/Vs$) | 6 | Hole mobility in valence-band extended states |
| $\varepsilon_{SiN}$ | 6.9 | Dielectric constant of the gate insulator |
| $d_a$ ($cm^{-3}eV^{-1}$) | $10^{16}$ | Peak value of Gaussian-distributed acceptor-like deep-gap states |
| $d_d$ ($cm^{-3}eV^{-1}$) | $10^{16}$ | Peak value of Gaussian-distributed donor-like deep-gap states |
| $E_a$ (meV) | 26 | Conduction-band-tail characteristic energy |
| $E_d$ (meV) | 55 | Valence-band-tail characteristic energy |
| $E_G$ (eV) | 1.8 | Band gap of a-Si:H |
| $g_a$ ($cm^{-3}eV^{-1}$) | $10^{21}$ | Density of states at $E_c$ |
| $g_d$ ($cm^{-3}eV^{-1}$) | $10^{21}$ | Density of states at $E_v$ |
| $L$ ($\mu m$) | 10 | Channel length |
| $d$ ($\mu m$) | 3 | Source/drain gate overlap |
| $R_c$ ($\Omega cm^2$) | 0.25 | Source/drain specific contact resistances |
| $R_t$ ($\Omega cm$) | 1.25 | $n^+$ a-Si:H film resistivity |
| $t_{a\text{-}Si:H}$ ($\mu m$) | 0.25 | a-Si:H film thickness |
| $t_{nSi}$ ($\mu m$) | 0.07 | $n^+$ a-Si:H film thickness |
| $t_{a\text{-}Si:N}$ ($\mu m$) | 0.35 | a-$SiN_x$:H (gate insulator) film thickness |
| $W$ ($\mu m$) | 60 | Channel width |

### 3.2.2 Temperature Effect on Amorphous Silicon Thin-Film Transistors

Transfer characteristics simulated at different temperatures ranging from 300 to 420 K at $V_{DS} = 0.1$ V show temperature-activated behavior, and the field-effect activation energy $E_{act}$ can be calculated from the Arrhenius plot, i.e., the slope of $\log(I_{DS})$ versus $1/T$ plot at a given $V_{GS}$.

An increase in the density of the deep-gap states causes only a threshold voltage shift and consequently no change of the $E_{act} - V_{GS}$ curve above threshold [20]. On the other hand, the conduction-band-tail has a significant effect on the activation energy curve. Figure 3.4 shows the $E_{act} - V_{GS}$ curves calculated for various conduction-band-tail slopes. The field-effect activation energy clearly increases with increasing density of conduction-band-tail states. An increase of the energy difference between the conduction-band edge and the Fermi level (at 0 K) can also be observed [21].

An experimental result is also given in Figure 3.4: Simulation cannot explain the experimental curve. This can be achieved by considering the temperature dependence of the source/drain series resistance. By adding temperature activated behavior of the S/D contact resistances and resistances of the $n^+$ a-Si:H layers, good fit can be obtained between the experimental and simulated field-effect activation energy curves [21].

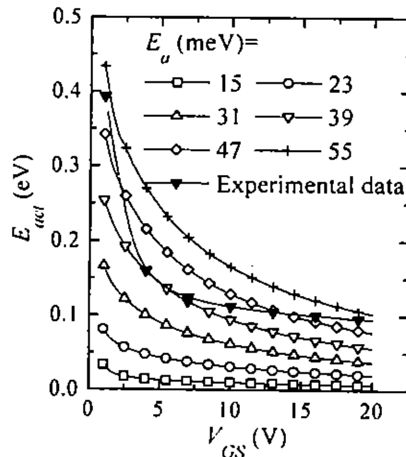


**FIGURE 3.4** Simulated evolution of the a-Si:H TFT field-effect activation energy for various conduction-band-tail slopes. (From Ref. 15.)

### 3.2.3 Amorphous Silicon Thin-Film Transistors Under Illumination

The numerical simulation program developed for the analysis of the a-Si:H TFT under illumination [22,23] is similar to the one described earlier, used in the dark. It solves simultaneously the three equations describing the steady-state conduction in semiconductors: the Poisson equation, electron and hole continuity equations, out of thermal equilibrium, using the Shockley–Read model for the carrier recombination rate. The amorphous silicon density-of-states is modeled by two exponential band tails and two Gaussian distributions of monovalent states, where the recombination process takes place. The program takes into account the a-Si:H density-of-states at the interfaces (a-Si:H/a-SiN$_x$:H and back-channel interfaces) and in the bulk of the semiconductor. The gate insulator is assumed to be ideal; i.e., there is no charge trapping or fixed charge present in the insulator layer. The TFT is illuminated from the source–drain side, and we assume that the whole a-Si:H layer is exposed to the light. The spatial resolution of the three-equation set is achieved over the whole a-Si:H TFT structure by defining an irregular 2D mesh, thinner at the interfaces between two different layers. For each set of input conditions (voltages and illumination conditions), we obtain, at every node of the 2D mesh, the values of the three unknowns: electrostatic potential and electron and hole Fermi potentials. These values allow us to deduce 2D maps of the physical parameters, such as the current densities, carrier densities, and electric field.

Figure 3.5 shows the TFT transfer characteristics simulated in the dark and under a uniform monochromatic illumination. We can distinguish both the a-Si:H TFT electron and hole threshold voltages, which delimit three main TFT operating regimes [24]:

(I) electron accumulation layer created at the a-Si:H/a-SiN$_x$:H interface;
(II) no accumulation layer;
(III) hole accumulation layer created at the a-Si:H/a-SiN$_x$:H interface.

In regime (I), the TFT drain current is associated with the drift diffusion of electrons in the accumulation layer (conduction channel). In regime (II), the TFT drain current results from the same mechanism as in regime (I), but the conduction occurs uniformly in the whole amorphous silicon layer (channel and bulk), since there is no carrier accumulation at the a-Si:H/a-SiN$_x$:H interface. Because the carrier densities in the whole amorphous silicon layer depend mostly on the light-induced generation and carriers recombination rates, in this regime the TFT drain current is sensitive to the amorphous silicon thickness and to the bulk density of states of amorphous silicon. In regime (III), the existence of the hole accumulation layer at the a-Si:H/a-SiN$_x$:H interface, in combination with

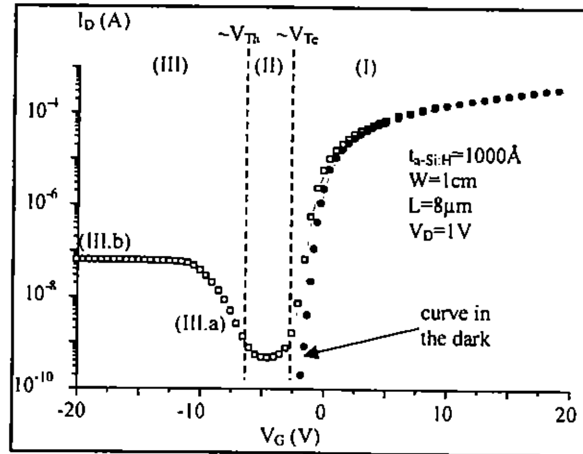


**FIGURE 3.5** Simulated a-Si:H TFT transfer characteristics under illumination and in the dark. (From Ref. 23, with permission from Society for Information Display.)

the $n+$ a-Si:H source/drain contact layers, results in a situation similar to two a-Si:H *pn* junctions located at the source and drain access areas. For a positive drain voltage, the source and drain junctions are, respectively, in the ON- and OFF-state.

We can actually distinguish two different conduction regimes within regime (III): In regime (III.a), the TFT current increases with the magnitude of the gate voltage, while it reaches a plateau in (III.b). The distinction between these two regimes depends on the relative importance of two different physical mechanisms: In regime (III.a), the drift diffusion of holes in the accumulation layer (conduction channel) is predominant, whereas in regime (III.b) the recombination of electrons and holes in the drain (OFF-state) *pn* junction depletion region is the most important. We should note that the importance of the source junction has been mentioned in [25], but we do not think that it is critical in regimes (III.a) and (III.b). Figure 3.6 shows the simulated variations of the electron and hole Fermi potentials along the usual TFT current path between the source and drain contacts. We can see that, in regime (III.a) (here for $V_G = -7.5$ V), the main variation of the Fermi potentials happens in the accumulation layer, where the drift diffusion of holes occurs. The conduction in this regime is similar to the conduction when the TFT is in the accumulation regime (gate voltage larger than the electron threshold voltage); however, in this regime the majority carriers are the holes

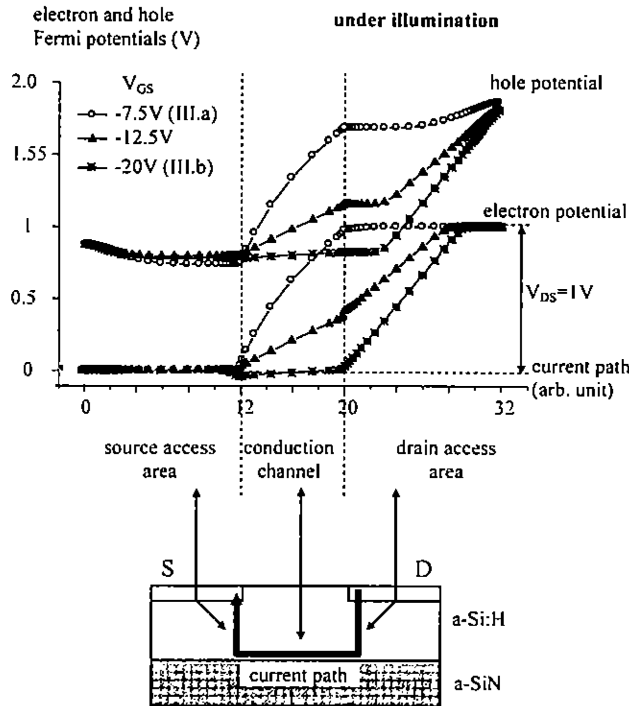


FIGURE 3.6 Simulated variations of the electron and hole Fermi potentials along the main TFT current path under illumination. (From Ref. 24.)

instead of the electrons. In contrast, in regime (III.b) (here for $V_G = -20$ V), the main variation of the Fermi potentials occurs in the drain *pn* junction depletion region, where the recombination of electrons and holes is taking place. Photogenerated current at the drain junction is the lowest [25] and is therefore the bottleneck in the process. Consequently, the a-Si:H TFT current depends only on the light-induced generation and recombination of electrons and holes in the drain *pn* junction depletion region. Actually, for high negative voltages, the recombination rate can be neglected, and the TFT current is therefore set only by the light-induced generation of electrons and holes (as in a photodiode case). This can explain why, in this regime, there is no longer any influence of the gate voltage (saturation phenomenon) or channel length on the TFT drain current as observed experimentally [23]. However, we should note that this saturation regime is not always reached for typical values of the gate voltage.

The parameters that influence the a-Si:H TFT drain current depend on the TFT operation regime to be considered. The electron and hole threshold voltages depend mostly on the amorphous silicon density-of-states associated with both the a-Si:H/a-$SiN_x$:H interface and the bulk a-Si:H; the difference between the two threshold voltages is higher for a larger density-of-states. In regime (II), the TFT drain current depends strongly on the amorphous silicon thickness but also on the a-Si:H bulk density-of-states; it increases with a-Si:H thickness and decreases with a-Si:H density-of-states. The drain current in regime (III.b) depends only on the light-induced generation of electron–hole pairs in the drain *pn* junction depletion region (between the drain contact and the a-Si:H/a-$SiN_x$:H interface); it increases with the illumination intensity and with the *pn* junction area.

## 3.3 AMORPHOUS SILICON THIN-FILM TRANSISTOR CHARACTERIZATION

### 3.3.1 Normalization of Thin-Film Transistor Characteristics

a-Si:H TFT transfer characteristics need to be normalized to accurately compare samples with different geometric parameters and/or different gate insulators [26]. First, in order to take into account the geometrical dependence of the TFT characteristics in the linear regime, we should use the normalized TFT conductance (in $\Omega^{-1}$) instead of the TFT drain current:

$$G = \frac{I_{DS}}{V_{DS} W/L} \tag{3.13}$$

where $V_{DS}$ is the source–drain voltage and $W$ and $L$ are the TFT channel width and length, respectively.

Then instead of the gate voltage, we should use the electrical charge induced by the gate voltage at the amorphous semiconductor/gate insulator interface (in $C/cm^2$):

$$Q_{\text{ind}} = V_{GS} \times C_i \tag{3.14}$$

where $C_i$ is the insulator capacitance per unit area. Alternatively, we can use $G/Ci$ versus $V_{GS}$ characteristics for the analysis of the TFT linear regime.

In the TFT saturation regime, we should use the normalized TFT current expressed by

$$I_{DS\text{norm}} = \frac{I_{DS}}{C_i W/2L} \tag{3.15}$$

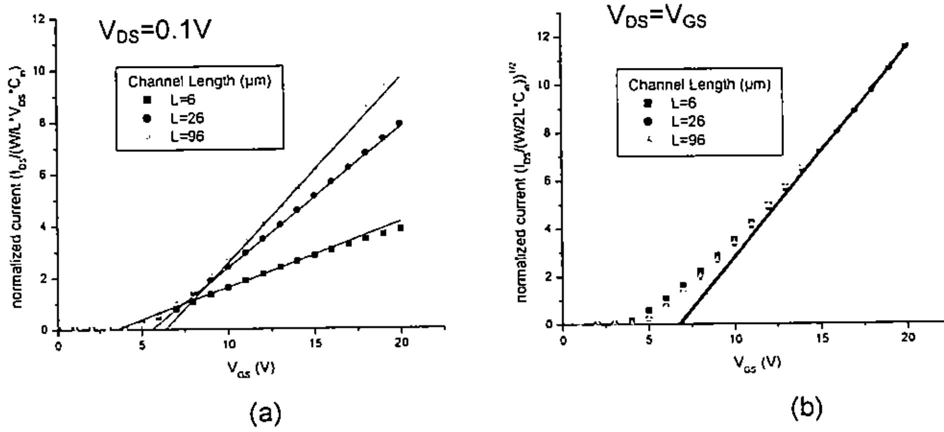


**FIGURE 3.7** Normalized a-Si:H TFT transfer characteristics and fitting used for extraction of the field-effect mobility and threshold voltage in the (a) linear and (b) saturation regimes.

Examples of normalized TFT characteristics in linear and saturation regimes are shown in Figure 3.7a and b, respectively.

### 3.3.2 Extraction of Thin-Film Transistor Electrical Parameters

The most basic TFT characterization involves the extraction of field-effect mobility, threshold voltage, and subthreshold swing. To obtain meaningful extracted TFT electrical parameters, the fitting range must be chosen carefully to ensure that devices with different geometry, gate insulator characteristics, or measurement conditions are compared in the same operating states, which do not necessarily occur at comparable gate voltage ranges.

In the linear regime, i.e., for low drain voltage, the TFT apparent field-effect mobility $\mu_{FE}$ and threshold voltage $V_T$ are deduced from the following equation, using the MOSFET gradual channel approximation:

$$\frac{I_{DS}}{V_{DS}C_i\ W/L} = \mu_{FE}\,(V_{GS} - V_T) \tag{3.16}$$

The fit of the experimental data to Eq. (3.16), as shown in Figure 3.7a, is performed around a fixed value of the normalized drain current $I_{DS}/(V_{DS}C_iW/L)$.

In the saturation regime (typically for $V_{DS} = V_{GS}$), the TFT field-effect mobility and threshold voltage are calculated from the following equation:

$$\frac{I_{DS}}{C_i W/2L} = \mu_{FE}(V_{GS} - V_T)^2 \tag{3.17}$$

The fit of the experimental data to Eq. (3.17), as shown in Figure 3.7b, is performed around a fixed value of the normalized drain current $I_{DS}/(C_i W/2L)$.

In addition, the normalized threshold voltage $V_T \times C_i$ should be used instead of the threshold voltage, to allow for comparison of devices with different gate insulator characteristics.

The subthreshold swing ($S$) is usually extracted from the TFT transfer characteristic in the subthreshold regime, using the following equation:

$$S = \left(\frac{d \log (I_D)}{dV_{GS}}\right)^{-1} \tag{3.18}$$

The fit of the experimental data to Eq. (3.18), as shown in Figure 3.8, is performed around a fixed value of $I_{DS}/(V_{DS}W/L)$. $I_{DS}/(V_{DS}W/L)$ can also be used in Eq. (3.18). From the value of the subthreshold slope, we can also calculate the equiva-

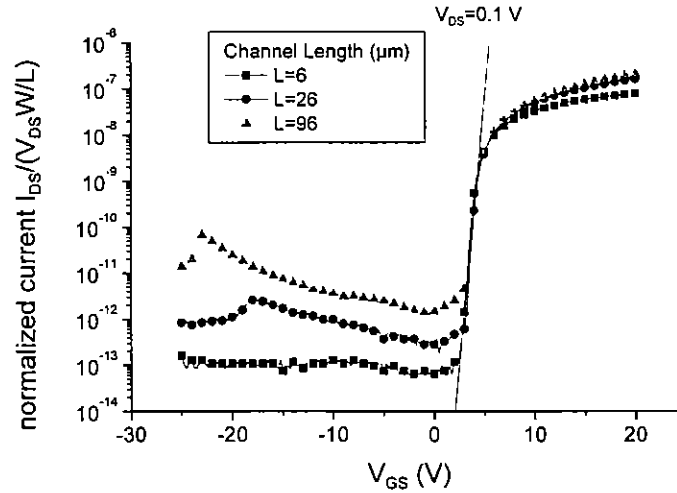


**Figure 3.8** a-Si:H TFT transfer characteristics and fitting used for extraction of the subthreshold swing.

lent maximum density-of-states that can be present at the amorphous semiconductor/gate insulator interface [27]:

$$N_{ss}^{max} = \left(\frac{S \log(e)}{kT/q} - 1\right)\frac{C_i}{q} \tag{3.19}$$

where $q$ is the electron charge, $k$ is the Boltzmann constant, and $T$ is the temperature. $N_{ss}^{max}$ can be used to compare devices with different gate insulator characteristics.

In the linear regime, the MOSFET equation predicts that, for low $V_{DS}$, a linear $I_{DS} - V_{GS}$ characteristic should be observed. However, $I_{DS} - V_{GS}$ characteristics of TFTs often exhibit a nonlinear behavior inconsistent with the predictions of the MOSFET gradual channel equation, as seen, for example, in Figure 3.9. This deviation from the ideal MOSFET behavior [9,16,28,29] has been associated with dispersive transport in a-Si:H [30]. More precisely, the device model was modified to include an additional parameter, $\gamma$, representative of the $I_{DS} - V_{GS}$ nonlinearity at low $V_{DS}$, as follows:

$$I_{DS} = M(V_{GS} - V_T)^{\gamma}\, V_{DS} \tag{3.20}$$

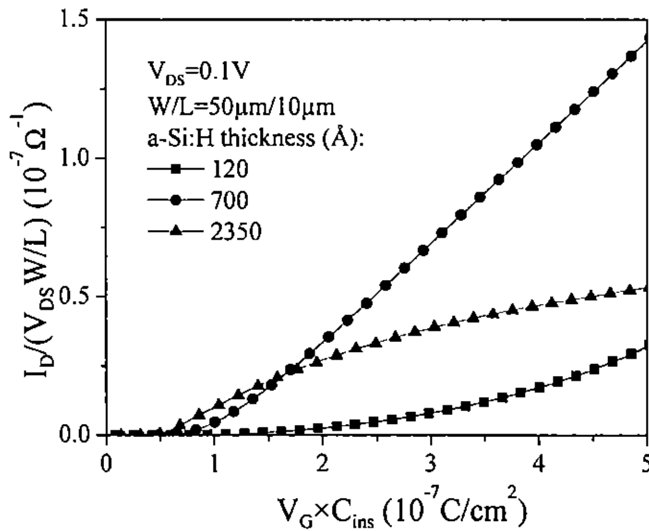


**FIGURE 3.9** a-Si:H TFT transfer characteristics in the linear regime exhibiting significant nonlinearity.

where $M = \mu_{FE}C_i\ (W/L)$. The physical signification of $\gamma$ is often given by

$$\gamma = 2\frac{T_0}{T} - 1 \tag{3.21}$$

where $T_0$ is the characteristic temperature of the amorphous semiconductor density-of-states distribution around the position of the Fermi level [16], i.e., typically the characteristic temperature of the conduction-band-tail states. The equation is valid for $T < T_0$. The nonideal situation of $\gamma > 1$ is associated with a high density of conduction-band-tail states, which can usually be attributed to variations of the Si–Si bond angles and distances in the amorphous semiconductor. However, $\gamma$ can be significantly underestimated in the case of nonnegligible source and drain series resistances [31].

We should note that, when the TFT parameter extraction is performed using Eq. (3.20), the unit of the term $\mu_{FE}C_i\ (W/L)$ is $A/V^{\gamma+1}$ (instead of $A/V^2$ as in the case of the MOSFET-based equation) and consequently depends on the value of $\gamma$. Therefore, to ensure proper comparison between samples with different $\gamma$-values, the TFT field-effect mobility and threshold voltage are extracted using Eq. (3.16), i.e., based on the MOSFET gradual channel approximation. Eq. (3.20) was used separately for the extraction of the $\gamma$-parameter only.

### 3.3.3 Thin-Film Transistor Source/Drain Series Resistances

The complete analysis of a-Si:H TFT electrical performance also involves the extraction of the TFT source and drain series resistances, the intrinsic field-effect mobility, and intrinsic threshold voltage. The intrinsic a-Si:H TFT parameters are representative of the electrical characteristics of the conduction channel itself without the influence of the parasitic series resistances. They can be extracted by the well-known transmission line method (TLM) [32,33] using a series of TFTs with different channel lengths measured at a low source–drain voltage, so we can neglect the space-charge-limited currents (SCLC) effect.

The total TFT ON-resistance is:

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch}\,L + 2R_{S/D} \tag{3.22}$$

where $r_{ch}$ is the channel resistance per channel-length unit and $2R_{S/D}$ is the total (source + drain) series resistances, respectively. Using Eqs. (3.16) and (3.22), we can express the total TFT ON-resistance $R_T$ as a function of the TFT apparent field-effect mobility and threshold voltage:

$$R_T = \frac{L}{\mu_{FE}\,C_iW(V_{GS} - V_T)} \tag{3.23}$$

The same equation applied to the ideal TFT (conduction channel only) lets us express the channel resistance as a function of the intrinsic mobility and threshold voltage, $\mu_{FEi}$ and $V_{Ti}$, which are representative of the conduction channel material, without the influence of the TFT series resistances:

$$r_{\text{ch}} = \frac{1}{\mu_{FEi}\, C_i W (V_{GS} - V_{Ti})} \tag{3.24}$$

The extraction of the TFT source and drain series resistances and intrinsic field-effect mobility and threshold voltages is rather straightforward using a series of TFTs with different channel lengths, as shown in Figure 3.10. We first plot the total TFT ON-resistance as a function of the TFT channel length for different gate voltages, ensuring that the TFT is in accumulation regime, and then we fit the experimental data to linear curves. This lets us obtain the TFT total series resistances ($R_S + R_D$) from the $y$-intercepts and the channel resistance per channel-length unit ($r_{\text{ch}}$) from the slopes. By plotting the reciprocal of $r_{\text{ch}}$ as a function of the gate voltage and, once again, determining its linear fit, the $x$-intercept gives the intrinsic threshold voltage $V_{Ti}$ and the slope yields the intrinsic field-effect mobility $\mu_{FEi}$ as indicated by Eq. (3.24).

The TFT series resistances are closely related to the overlap between source (or drain) contact and gate contact. The TFT drain current does not usually flow

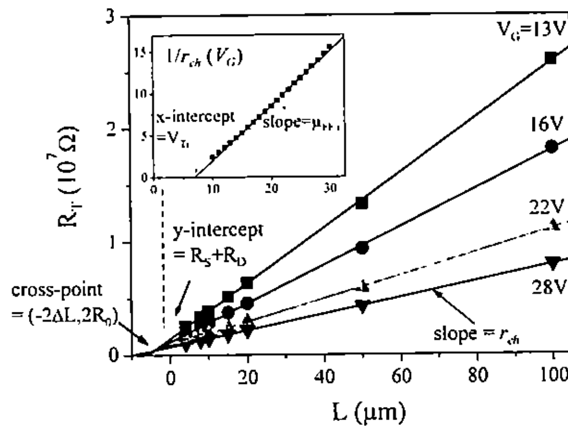


**FIGURE 3.10** Illustration of the transmission line method used to extract the S/D series resistances and the a-Si:H TFT intrinsic parameters. The total ON-resistance $R_T$ has been plotted as a function of the TFT channel length for different gate voltages. The inset shows the evolution of $1/r_{\text{ch}}$ with the TFT gate voltage. Symbols: experimental results; solid lines: linear fits. (Adapted from Ref. 26)

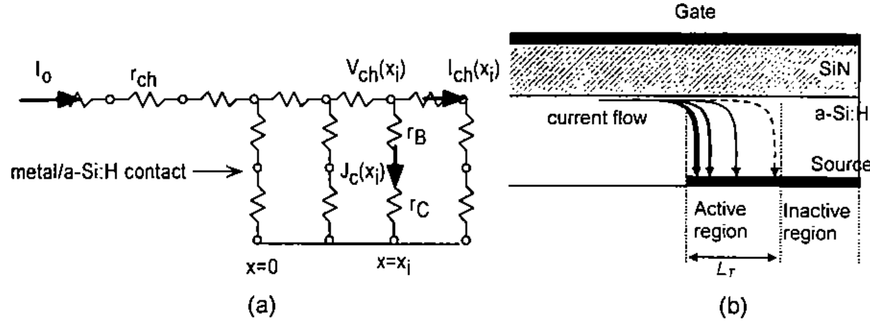


FIGURE 3.11 (a) Equivalent circuit near and above the a-Si:H TFT source electrode. (Adapted from Ref. 39.) (b) Representation of the characteristic length $L_T$. (From Ref. 23.)

through the whole source or drain contact but is more likely limited to a specific area of the contact [34–36]. More precisely, we can define the TFT characteristic length ($L_T$) representing the dimension (along the source–drain axis) of the effective contact area. Figure 3.11 illustrates the top-gate a-SI:H TFT cross section and simplified schematic circuit diagram at the source contact. At the source-electrode side, the change of the channel current above the source electrode can be expressed as

$$\frac{dI_{ch}(x)}{dx} = -WJ_c(x) \tag{3.25}$$

with

$$J_C(x) = V_{ch}(x)/r_{Ceff} \tag{3.26}$$

and

$$r_{Ceff} = r_B + r_C \tag{3.27}$$

where $I_{ch}(x)$ is the horizontal current in the channel (a-Si:H/a-SiN$_x$:H interface) at position $x$, $J_c(x)$ is the vertical current density at position $x$, $V_{ch}(x)$ is the electrical potential in the channel at position $x$, and $r_B$ and $r_C$ are the vertical bulk and contact resistivity (in $\Omega$-cm$^2$), respectively.

The variation of $V_{ch}(x)$ along $x$ can be expressed as

$$\frac{dV_{ch}(x)}{dx} = -I_{ch}(x)r_{ch} \tag{3.28}$$

Combining Eqs. (25), (26), and (27), we have

$$\frac{d^2V_{ch}(x)}{dx^2} = \frac{1}{L_T^2} V_{ch}(x) \tag{3.29}$$

with

$$L_T^2 = \frac{r_{Ceff}}{W r_{ch}} \tag{3.30}$$

where $L_T$ is the characteristic length of the source (drain) series resistance at a fixed $V_{GS}$.

The boundary conditions for Eq. (2.28) are

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=0} = -I_0 r_{ch} \tag{3.31}$$

and

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=d} = 0 \tag{3.32}$$

where $I_0$ is the total TFT drain-to-source current.

We can solve Eq. (3.29) for $V_{ch}(x)$ analytically:

$$V_{ch}(x) = I_0 r_{ch} L_T \frac{\cosh[(x - d)/L_T]}{\sinh(d/L_T)} \tag{3.33}$$

The series resistance $R_{S/D}$ (in ohms) at the source or drain contact can then be expressed as

$$R_{S/D} = \frac{V_{ch}(x = 0)}{I_0} = r_{ch} L_T \coth\left(\frac{d}{L_T}\right) \tag{3.34}$$

and

$$L_T = \frac{R_{S/D}}{r_{ch} \coth(d/L_T)} \tag{3.35}$$

The values of $R_{S/D}$ and $r_{ch}$ are determined experimentally from Eqs. (3.22) and (3.24), respectively. Therefore, $L_T$ can be calculated by solving Eq. (3.35) numerically. Furthermore, if $d/L_T >> 1$, Eq. (3.35) can be reduced to

$$L_T = \frac{R_{S/D}}{r_{ch}} \tag{3.36}$$

and from Eq. (3.30) we can obtain the effective contact resistance:

$$r_{Ceff} = W L_T^2 r_{ch} = \frac{W R_{S/D}^2}{r_{ch}} \tag{3.37}$$

It can be shown that, as expected for a-Si:H TFTs, $r_{Ceff}$ and $L_T$ vary with $V_{GS}$ in