

# **Ultrafast DOD-N Logic Gates for Router Applications**

*Mohammed N. Islam*

*Department of Electrical Engineering and Computer Science*

*University of Michigan at Ann Arbor*

*Ph: (734)647-9700; Email: mni@eecs.umich.edu*

## **Abstract**

The University of Michigan requests seed funding to research and demonstrate ultrafast, DOD-N logic functions using a platform technology consisting of a semiconductor optical amplifier Mach-Zehnder interferometer. By using a symmetric structure with SOA's biased at transparency and counter-propagating signals and clock, all of the requirements for a DOD-N logic gate can be satisfied. This configuration of the SOA-MZI can serve as the key enabling building block for modules such as 3R regenerators or wavelength converters, or for DOD-N sub-systems such as label swapping, header processing or error checking.

As a subset of the original SAMMI Consortium proposal that was submitted at the end of May, 2003 to DARPA, the University of Michigan (UM) requests seed funding from DARPA to demonstrate and integrate the platform logic gates. The work will focus on fundamental and device aspects of the logic gate platform, along with their potential applications in modules for logic operations, 3R regeneration and wavelength conversion. For a sufficient funding level and duration of the project, the logic gates can also be bench-top integrated into DOD-N sub-systems, such as label swapping, header processing and error checking.

### **A. DOD-N Logic Gates (device platform)**

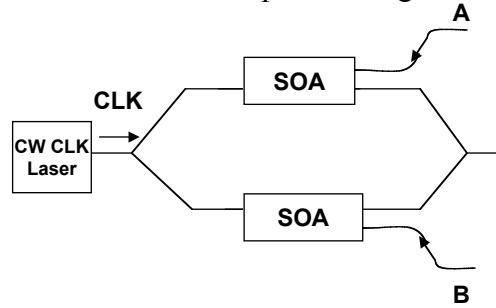
We propose a semiconductor optical amplifier Mach-Zehnder interferometer (SOA-MZI) building block for all the logic operations, with a particular emphasis on XOR functionality. Beyond the logic functions, the next section describes how the same device platform can be used for modules such as 3R regeneration and wavelength conversion. Finally, the last few sections describe how the device platform may be used for DOD-N sub-systems, including label swapping, header processing and error checking.

The requirements on DOD-N logic gates include:

- three-terminal devices (clock – CLK – and signals are separable)
- cascadable (same wavelength output, minimize pulse distortion)
- polarization independent (input is random polarization)
- regenerative logic (output is new CLK photons, with either 2R or 3R clean-up)
- ultrafast operation (operate at speeds of 100Gb/s or more and avoid inter-symbol interference (ISI) or pattern dependence)
- high contrast ratio (low off state, high on/off contrast)
- Boolean complete (NOT, AND, XOR, etc.)

In the design below, we meet all of these requirements using a particular configuration of the SOA-MZI. In particular, by using counter-propagating CLK and signals, we achieve three-terminal, cascadable and polarization independent operation. Regenerative operation is achieved by replacing the incoming photons with new photons from local CLK source. Ultrafast operation is achieved by using a symmetric structure and biasing at the gain transparency point.

Finally, high contrast can be achieved by proper balancing of the SOA-MZI for a low null state, and the SOA-MZI turns out to be a Boolean complete configuration.



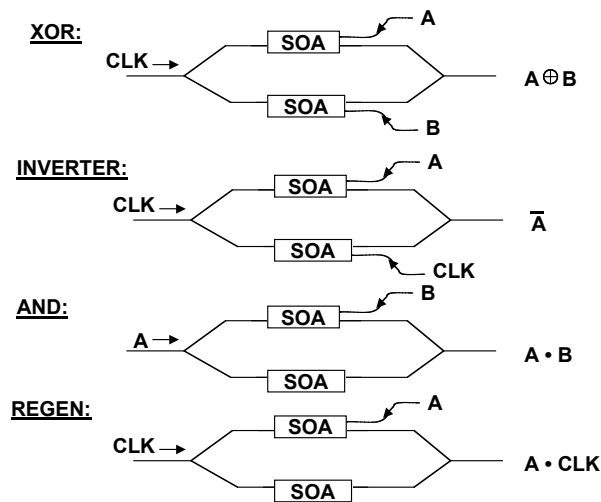
**Figure A.1** Ultrafast symmetric SOA logic gate configuration for bit level processing

The configuration for the SOA-MZI logic gate for bit level processing is illustrated in Fig. A.1. Two SOA's are placed symmetrically in an integrated MZI, and the structure is biased to achieve a null output when signals A and B are absent. The two signals are counter-propagating to the CLK input, which is shown as a CW laser at the same wavelength as A and B for the logic gate operations. When either A or B are on, then they change the phase in one arm of the MZI through cross-phase modulation, which imbalances the interferometer and leads to an output. On the other hand, when both A and B are on, the cross-phase modulation phase shift is equal in the two MZI arms, resulting in a null output. Hence, the structure's basic operation is that of an XOR gate [1-5].

The structure of Fig. A.1 achieves all of the logic gate requirements. By using the counter-propagating geometry, the CLK and signals can be at the same wavelength [6, 7], and the signals can be separated out by using an isolator or circulator at the CLK input. The counter-propagating geometry has also been shown to be polarization independent, if the SOA's used are polarization independent [5-7]. The logic gate is regenerative because the outgoing photons are from the local CLK source, and the incoming signal photons are not reused. This means that distortions do not accumulate as several logic gates are cascaded. In addition, the SOA-MZI acts as an OSNR booster or a 2R-type regenerator for the incoming signals [1, 8, 9], since the transfer function of the MZI is a sine-squared, nonlinear operation. For example, noise at low intensity is preferentially suppressed since the sine-squared function is quadratic at low intensities, and then the signal level can be biased to be in the more-or-less linear regime for high throughput. In fact, if the signal energy is close to that required for a  $\pi$ -phase shift, then the logic gate also performs a limiting function (i.e., close to the top of the sine-squared function the output is limiting, thereby suppressing intensity fluctuations on the signal).

Ultrafast operation (up to 160Gb/s) can be achieved by using a symmetric structure and biasing the SOA's at transparency. By using a symmetric structure the slow nonlinearity is common mode and cancels out, leading to switching based only on the fast nonlinearity effects. For example, the group at the University of Michigan (UM) has demonstrated 100Gb/s optical switching using a symmetric semiconductor switch based on cross-phase modulation from the picosecond nonlinearity in SOA's. For those experiments we used an SOA in the center of a nonlinear optical loop mirror, and we were able to avoid cross-talk from adjacent control pulses while obtaining switching due to the picosecond nonlinearity. In particular, the switching energy was 8pJ, switching window as 3psec, the contrast ratio was 25:1 for AND-gate operation, and the switched out pulses were cascable [10, 11]. With an integrated configuration and better SOA technology, we expect to lower the switching energy closer to a picojoule.

Ultrafast performance of the SOA-MZI can be obtained by biasing the SOA's at transparency, thereby avoiding bit-pattern dependence and ISI because no net carriers remain after the pulses pass through. As an example, the UM group demonstrated a 100Gb/s AND-gate with 2psec recovery time and 4pJ switching energy by using an InGaAsP SOA at transparency in a nonlinear optical loop mirror [10, 11]. We also showed that the fast nonlinearity arises from carrier heating and two-photon absorption, and for proper operation the control pulses should be longer than the length of the SOA (e.g., a 500 micron SOA is about 5psec long). Moreover, the Heinrich-Hertz Institute in Germany has reported 160Gb/s operation of a DOD-N demultiplexer and add/drop multiplexer using an SOA-based ultrafast nonlinear interferometer (UNI) with the SOA biased at gain transparency [12, 13]. They achieve a 1pJ switching energy, and they note that at gain transparency the disturbing pattern effects caused by the gain recovery in the SOA are avoided. However, the UNI configuration is strongly polarization dependent, whereas the configuration of Fig. A.1 is polarization independent.



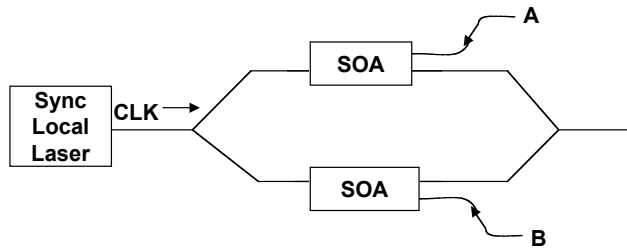
**Figure A.2** Different configurations show the versatility and Boolean completeness of the SOA-MZI

The different configurations of Fig. A.2 show the versatility and Boolean completeness of the SOA-MZI. As described above, the configuration with A and B inputs corresponds to an XOR functionality. If the CLK is input into one arm, then the device also acts as an inverter. Moreover, if the two signals are fed into the two directional ports, then an AND gate functionality is achieved. Finally, with the CLK replaced by pulses, the gate acts as a buffer switch or regenerator, which is further described below.

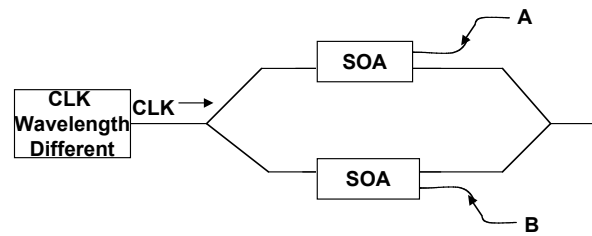
## **B. 3R regenerator and Wavelength Conversion (modules)**

For the logic operations in Fig. A.1, a CW CLK laser is used. This is desired because DOD-N label swapping and other functions can be transparent to the packet bit rate and format. Also, a 2R regenerative (re-shaping, re-timing) or OSNR boosting can occur because of the nonlinear sine-squared transfer function of the MZI. However, if 3R regeneration is required as in the output interface, then it is difficult to remain transparent to the packet format. The same SOA-MZI structure can be used as a 3R regenerator by replacing the CW CLK by a sync laser source CLK (Fig. B.1) [6, 7]. The sync laser source is assumed to provide a pulsed or modulated output that is synchronized to the incoming data stream using a phase lock loop. Therefore, the sync laser source provides the third R of the 3R, namely retiming.

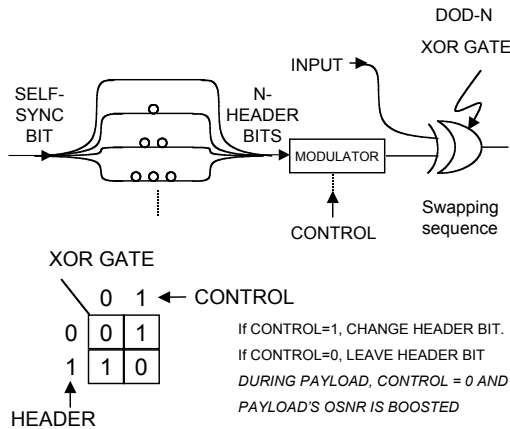
The logic operations and 3R regeneration have thus far assumed that the CLK laser is at the same wavelength as the incoming data. However, if simultaneous wavelength conversion is desired, then the CLK laser can be at the selected output wavelength (Fig. B.2). If the wavelength conversion is to be 2R, then the CLK can be CW, or if the wavelength conversion is to be 3R, then the CLK needs to be a sync laser source. Since the output wavelength can vary and will be determined most likely by the control and management plane to minimize contention in the network, it is desirable that the laser source be tunable.



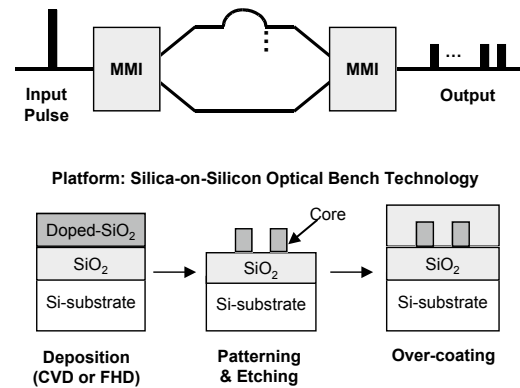
**Figure B.1** The SOA-MZI structure can be used as a 3R regenerator by replacing the CW CLK by a sync laser



**Figure B.2** For wavelength conversion, the SOA-MZI can be used with a CLK at a different wavelength



**Figure C.1** DOD-N label swapping can be performed efficiently using a simple XOR gate



**Figure C.2** Replication of the self-sync trigger bits using integrated optical delay lines

### C. DOD-N Label Swapping (sub-system)

The DOD-N label swapping can be performed efficiently using a simple DOD-N XOR gate [14] (Fig. C.1). To simplify the synchronization as well as to desensitize to inter-packet jitter, the self-sync bit from the self-sync trigger is replicated for the duration of the label. A modulator can then be used to encode the swapping sequence on the new label bits. As Fig. C.1 shows, the XOR gate functionality is such that if the swapping sequence is “1”, then the label bit will be changed. For example, say that the incoming label is 110010 and the desired output label is 100111. Then, the swapping sequence should be 010101, where the 1’s are used to flip the existing label bits. Also, during the packet the swapping sequence is set to zero, so the XOR gate does not alter the packet sequence. Some of the advantages of this DOD-N label swapping technique are:

- wavelength conversion is not required and a time guard band is not required between the label and packet
- label swapping is transparent to the packet format and bit rate
- the DOD-N XOR gate acts as an OSNR booster for the packets, providing a 2R functionality
- the label swapping is always synchronized to the packet, since the processing bits are derived from the beginning of the packet.

The replication of the self-sync trigger bits can be achieved using integrated optical delay lines (Fig. C.2). For example, a multi-mode interference coupler can be used as the multiplexer and demultiplexer, since it has a broad bandwidth and high fabrication tolerance. Then, waveguides can be formed for each of the label bits, where the delay between the bits corresponds to 25psec (~5mm in length) for 40Gb/s labels or 6.25psec (~1mm length) for 160Gb/s labels. This photonic integrated circuit can be formed using silica-on-silicon optical bench technology, which is fiber compatible (low insertion and propagation loss) and can be fabricated using well-established semiconductor processing techniques.

#### D. DOD-N Header Processing (sub-system)

Similar to the label swapping, the DOD-N header processing can be accomplished using logic gates and replication of the self-sync trigger. For the processing, the output from the self-sync trigger is replicated into an all “1” header to check for an empty packet and the inverted local address to compare with the incoming label. Since the bits are only on during the label or header, the processing is limited to the duration of the label. These inputs are fed to the cascaded logic gates of Fig. D.1, consisting of a DOD-N inverter followed by an XOR-gate. A threshold detection scheme is used, meaning that if all of the output bits are zeros over the label length, then the output level falls below some threshold and a positive decision is reached. The packet label is first processed by an inverter, and the output is all zero only if the packet is an empty packet (i.e., an empty packet is assigned an all one header). The threshold detector at the inverter output signals an empty packet in this case. Otherwise, the inverted label is compared with the bar of the local address in an XOR gate, whose output is all zero only if every bit matches. Therefore, the threshold detector at the XOR gate output signals if the label matches the local address. For simple protocols such as in a ring architecture, as few as only two levels of logic may be required. However, a very powerful aspect of the proposed approach is that further levels of cascaded logic can be used for more complicated protocols or header processing functions.

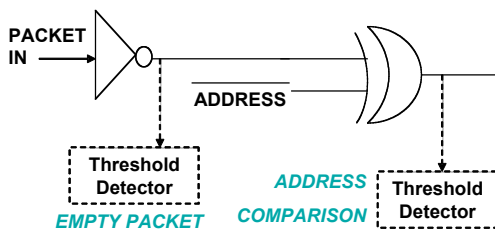


Figure D.1 DOD-N header processor

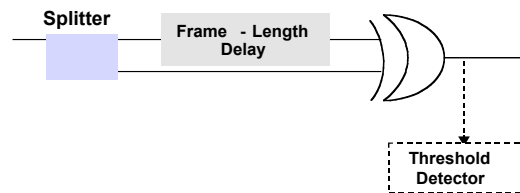


Figure E.1 DOD-N error checker

#### E. DOD-N Error Checking (sub-system)

To implement a simple error check, the frame label can be repeated after the original packet. The scheme in Fig. E.1 is used, where the label at the beginning is compared with the

label at the end of the packet. The two copies are compared using an DOD-N XOR gate, and an all zero output is achieved only when the two labels match, which is signaled by the threshold detector. If there is a mismatch in address or label, a warning is sent to the edge router that the data may be corrupted.

## F. Summary

In summary, a configuration of the SOA-MZI that can serve as an ultrafast, DOD-N platform technology is proposed. All requirements for DOD-N logic gates can be satisfied by using a symmetric MZI structure with SOA's biased at transparency and with counter-propagating signals and clock. By making the clock source a synchronized laser source or a different wavelength laser, either 3R regeneration or wavelength conversion modules can be implemented. Furthermore, the DOD-N logic gates can serve as a key enabling building block for DOD-N sub-systems such as label swapping, header processing or error checking. The U-M requests seed funding to investigate fundamental and device aspects of the platform logic gates, along with some applications to DOD-N modules and sub-systems.

## References

1. M.N. Islam, "Ultrafast Fiber Switching Devices and Systems," *Cambridge University Press, Cambridge, UK*, Aug. 1992.
2. A. Lattes, H. A. Haus, F. J. Leonberg, E. P. Ippen, "An Ultrafast All-Optical Gate", *IEEE J. Quantum Electron.*, Vol.19, pp. 1718-1723, Nov. 1983.
3. T. Fjelde, D. Wolfson, A. Kloch, B. Dagens, A. Coquelin, I. Guillemot, F. Gaborit, F. Poingt, and M. Renaud, "Demonstration of 20 Gbit/s all-optical logic XOR in integrated SOA-based interferometric wavelength converter", *Electron. Lett.*, vol. 36, pp. 1863-1864, Oct. 2000.
4. K. E. Stubkjaer, "Semiconductor Optical Amplifier-Based All-Optical Gates for High-Speed Optical Processing," *IEEE Journal Selected Topics of Quantum Electronics*, vol. 6, pp. 1428-1435, Nov/Dec. 2000.
5. J. H. Kim, Y. M. John, Y. T. Byun, S. Lee, D. H. Woo, and S. H. Kim, "All-Optical XOR Gate Using Semiconductor Optical Amplifiers Without Additional Input Beam," *IEEE Photonics Technology Letters*, vol. 14, pp. 1436-1438, Oct. 2002.
6. S. Fischer, M. Dulk, E. Gamper, W. Vogt, E. Gini, H. Melchior, W. Hunziker, D. Nessel, and A. D. Ellis, "Optical 3R regenerator for 40 Gb/s networks," *Electronics Letters*, vol. 35, pp. 2047 -2049, Nov. 2000.
7. O. Leclerc, B. Lavigne, D. Chiaroni and E. Desurvire, "All-Optical Regeneration: Principles and WDM Implementation," *Optical Fiber Telecommunications, Volume IVA*, Elsevier Science, Academic Press, San Diego, CA, 2002.
8. M.N. Islam, Patent Pending, "SNR Booster for WDM Systems," *United States Patent and Trademark Office*, Wash. D.C., 2001.
9. D. J. Blumenthal, B. E. Olsson, G. Rossi, T. E. Dimmick, L. Ran, M. Masanovi, O. Lavrova, R. Doshi, O. Jerphagnon, J. E. Bowers, V. Kaman, L. A. Coldren, and J. Barton, "All-optical label swapping networks and technologies," *Journal of Lightwave Technology*, vol. 18, pp. 2058-2075, Dec. 2000.

10. Y. H. Kao, T.J. Xia, G.A. Nowak, A.A. Said, M.N. Islam and G. Raybon, "100 Gb/s optical switching using a symmetric semiconductor switch," submitted to *Photonics Technology Letters*, Nov. 1998. (also Y.H. Kao, "Ultrafast Optical Switching Using Semiconductors for High-Speed Communication Systems," *PhD Physics Thesis, University of Michigan*, 1998)
11. Y. H. Kao, T. J. Xia, M. N. Islam, and G. Raybon, "Limitations on ultrafast optical switching in a semiconductor laser amplifier operating at transparency current," *Journal of Applied Physics*, vol. 86, pp. 4740-4747, Nov. 1999.
12. C. Schubert, S. Diez, J. Berger, R. Ludwig, U. Feiste, H. G. Weber, G. Toptchiyski, K. Petermann, and V. Krajinovic, "160-gb/s all-optical demultiplexing using a gain-transparent ultrafast-nonlinear interferometer (GT-UNI)," *IEEE Photonics Technology Letters*, vol. 13, pp. 475-477, May 2001.
13. C. Schubert, C. Schmidt, S. Ferber, R. Ludwig, and H. G. Weber, "Error-free all-optical add-drop multiplexing at 160 Gbit/s," *Optical Fiber Communication Conference*, PD-17, Atlanta, GA, USA, Mar. 2003.
14. T. Fjelde, A. Kloch, D. Wolfson, C. Janz, A. Coquelin, I. Guillemot, F. Gaborit, F. Poingt, B. Dagens, and M. Renaud, "Novel scheme for efficient label-swapping using simple XOR gate," *European Conference on Optical Communication (ECOC)*, Paper no. 10.4.2, pp. 63-64, Munich, Germany, Sept. 2000.