

# High Speed Processor-Memory Interfaces

Ph.D. Thesis Proposal

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**Abstract- High performance I/O interface design is becoming a very important research area within VLSI. Increases in microprocessor clock frequencies have dramatically outpaced increases in I/O bandwidth, resulting in a bottleneck between processors and memory. This proposal discusses the issues relevant to high speed interface design. Studies are described that will allow for the design of a high speed, low power processor-memory interface. The interface is intended to be used in a complementary gallium arsenide (CGaAs), multichip module implementation of the PowerPC architecture. The goal of the work is to design an interface that maximizes bandwidth and noise immunity, minimizes power and meets the needs of future microprocessors.**

## 1. INTRODUCTION

Modern microprocessors operate at very high clock frequencies, due to scaling in VLSI technology. These microprocessors require very high memory bandwidth in order to utilize resources efficiently. Current I/O interfaces do not provide enough bandwidth, and the result is a significant bottleneck between processors and memory [1],[2]. While processor speeds have increased at a rate of 40% per year, off-chip signaling rates have scaled more slowly, at a rate of approximately 14% per year [3]. Also, the number of available pins are increasing at a rate of approximately 12% per year [3], rapidly outpaced by the amount of on-chip functionality. The bandwidth gap is growing at 33% per year [3].

Recent trends in both computer architecture and applications are exacerbating the problem. While processor speeds have increased dramatically, DRAM speeds have increased at only 7% per year

[4]. This has led to architectural techniques designed to reduce or tolerate latency. However, many of these techniques require high peak bandwidth. For example, hardware prefetching [5], stream buffers [6], and software directed prefetching [7] trade increased bandwidth for reduced latency. Multi-issue implementations and multiprocessors also require very high bandwidth to increase overall throughput. Popular applications are becoming more and more graphics intensive. These applications tend to have very little locality, leading to even higher bandwidth requirements.

The digital signalling problem is illustrated in Fig. 1 [8]. Two chips must exchange data over a multichip module (MCM) or printed-circuit board (PCB) at a high rate through a finite number of signal channels. The transfer rate is limited by noise in the electrical environment. Prominent sources of noise include transmission line reflections, power supply disturbances, capacitive coupling and processing variations. Many of the noise sources are signal dependent and caused by parasitic resistance, capacitance, and inductance (illustrated in Fig. 1).

Conventional digital interface circuits have tended to overpower noise rather than reject it. This has led to the generation of more noise and higher power dissipation. Internal power supply voltages are decreasing by approximately 15% a year [3]. Currently, IC's operating with 2V supplies are not uncommon [9],[10]. This has resulted in low power cores. However, chips still require a 3.3V supply voltage for I/O. The interface voltage will eventually scale to 2V, seriously compromising I/O noise

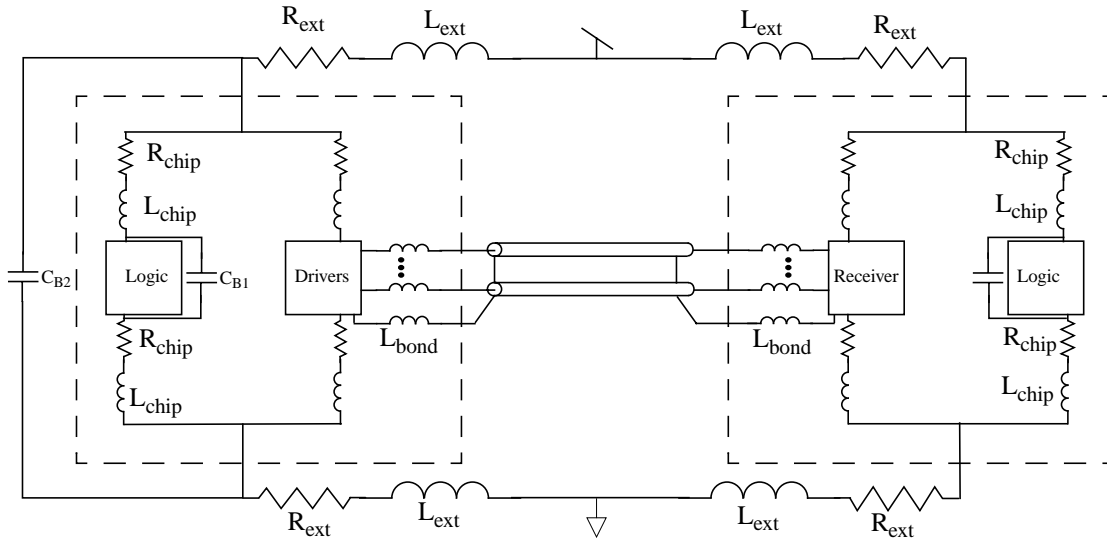


Fig. 1. Two chips exchange data over signal pins connected by transmission lines [8]

margins. New circuits will be required in the near future to accommodate low supply voltages in the presence of noise.

At first glance, it appears that the obvious solution to the I/O bottleneck is to increase the number of pins using an advanced packaging approach. This makes possible high bandwidth connections to the memory subsystem. However, high signal counts imply higher I/O power, and a noisier environment. Therefore, advanced packaging can only be used effectively if new transceivers are designed that filter out noise, and consume little power.

Conventional clock and data recovery approaches leave the interface susceptible to timing noise. Delay-locked-loops (DLL's) are typically used to generate a latching edge at the receiver that is  $90^\circ$  out of phase with the incoming data. This maximizes the probability of meeting both the set-up and hold constraints at the receiver. However, noise inherent to the transistors and on the power rails causes the sampling edge to stray from its ideal location. This noise is becoming an increasingly larger part of the bit time, degrading the interface. New approaches are required that are robust and minimize jitter and skew.

This proposal will address the issues involved in high speed interface design including:

- *sources of noise and how they are managed,*
- *termination strategies,*
- *clock and data recovery schemes,*
- *low-jitter delay-locked-loop design,*
- *electrostatic discharge protection circuits.*

These issues will be related to the design of high speed interfaces for a multichip module implementation of the PowerPC architecture.

## 2. OVERVIEW OF APPLICATION

Researchers at the University of Michigan are developing a multichip complementary gallium arsenide (CGaAs) implementation of the PowerPC architecture, known as PUMA [11]. The project is exploring many facets of high clock rate microprocessors.

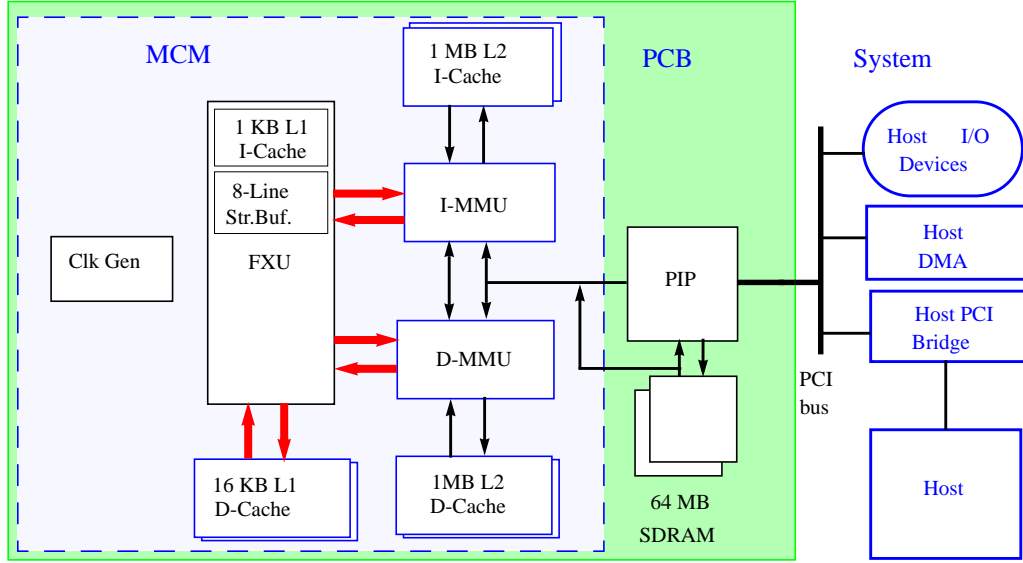


Fig. 2. Overview of PUMA Architecture

## 2.1 SYSTEM ARCHITECTURE

The PUMA system architecture is illustrated in Fig. 2. The limited integration levels of CGaAs force a partitioning of the processor onto several VLSI chips and a small clock generator chip. The CPU chip interfaces directly with the 4 data cache chips and the memory management chips. The characteristics of CGaAs (short gate delay and low integration levels) dictate that the datapaths and control be simple. Since the integration level will not support much parallelism, the processor's performance must come from high clock frequency.

## 2.2 PACKAGING APPROACH

A flip-chip, array-pad packaging approach will be implemented to increase bandwidth to memory by providing high I/O counts [12]. IC's having peripheral pads can be flip-chip mounted, but they require wide on-chip power rails to assure stable voltages in the core, and they usually have long interconnect routes from the core to the bonding pads. Conventional flip-chip array packaging methods redistribute signals from the periphery to an array of bumps covering the chip surface; while there are some advantages to these approaches, the

power distribution situation has not been helped, and interconnect is made even longer.

Fig. 3 is a high-level cross-section of the proposed array-pad packaging approach [13]. CGaAs circuits are flip-chip mounted on the MCM, with a heat sink attached to the back of these chips. Signal I/O will be distributed across the chip on fine-pitch gold bumps, which will connect to receivers, drivers, and ESD protection modules. Power pads will provide V<sub>dd</sub> and Ground for each module, reducing the size of power rails. Additional thermal vias will be added as needed.

MCM-D technology (MMS-D500) is considered a good candidate for PUMA's MCM for several reasons:

- The signal layers are low resistance copper and the dielectric is polyimide ( $\epsilon_r=3.5$ ),

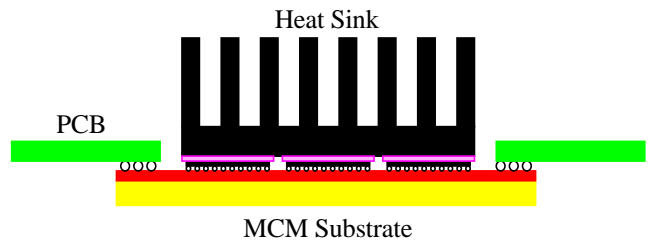


Fig. 3. Packaging Approach

- The technology offers low power-ground plane inductance and a distributed power-ground decoupling capacitance of  $\sim 0.8 \text{ nF/cm}^2$ ,
- It provides high wiring capacity to accommodate high pin count and fine pad pitch VLSI chips.

The technology offers five layers: pad, metal-3 (upper signal) interconnect, metal-2 (lower signal) interconnect, power plane and a ground plane which consists of an aluminum substrate.

### 2.3 SEMICONDUCTOR TECHNOLOGY

The chips will be designed using Motorola's  $0.5 \mu\text{m}$  CGaAs process [14]. A CMOS prototype will also be fabricated (through the MOSIS service). The CGaAs process has  $0.36$  and  $-0.5$  V thresholds for the n and p devices, respectively. The transconductance of the p device is approximately a factor of 4 less than that of the n device. The process corners used in simulations are  $\sigma_{V_{Tn}}=30$  mV and  $\sigma_{V_{Tp}}=60$  mV. Fig. 4 shows a schematic cross section of the CGaAs devices.

The AlGaAs layer serves as an insulator (analogous to  $\text{SiO}_2$  in MOS devices). The channel consists of a layer of undoped InGaAs. N and p channel source and drain implants are self-aligned to the gates. The process results in transistors which have very high transconductance. However, several process related issues exist which greatly influence design, two of which will be described here.

One issue is gate leakage current which has been observed in both the transient- and steady-state.

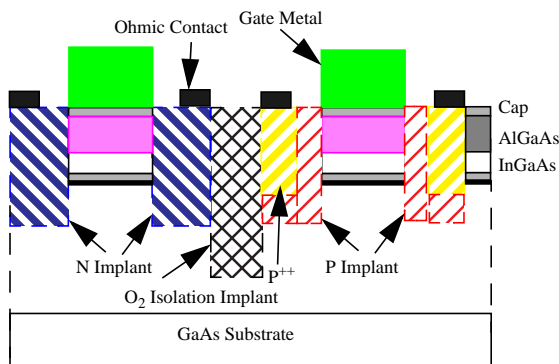


Fig. 4. CGaAs Cross-section

The insulating AlGaAs layer is non-ideal and the Schottky gate leaks when gate voltages exceeding 1 V are applied.  $22 \mu\text{A}$  of gate leakage current has been observed for a  $1 \times 10 \mu\text{m}$  n-channel device ( $V_{GS}=1.5$  V). Gate leakage leads to high static power dissipation and wider power rails. Its effects must also be carefully considered when designing analog circuits and I/O receivers.

Another issue which impacts circuit design is subthreshold current. Very low subthresholds have been achieved for  $1 \times 10 \mu\text{m}$  devices. However, for  $0.5 \mu\text{m}$  gate length devices, currents of  $0.5 \mu\text{A}$  have been reported [16]. This is caused by source/drain implant straggle effects. Subthreshold conduction is of concern in circuits where feedthrough effects are of concern (i.e., pass transistor latches).

### 3. HIGH SPEED INTERFACE DESIGN ISSUES

This section will discuss issues involved in high speed digital interface design.

#### 3.1 NOISE

Understanding what causes noise is extremely important to the interface designer. Noise sources must be minimized and managed in order to ensure proper system operation.

##### 3.1.1 Transmission Line Behavior

An electrical model of a uniform transmission line having inductance  $L$ , resistance  $R$ , capacitance  $C$ , and transconductance  $G$  (all per unit length) is shown in Fig. 5 [17]. The inductor resists changes in current by generating a reverse electromotive force. This limits the amount of current that can charge up a length of a capacitive line at any given time, thereby limiting how fast a wave can travel.

Transmission line behavior becomes significant when the rise time,  $T_R$ , of a signal is comparable to the transmission line time-of-flight delay  $T_{FL}$ . The rise time is defined as the time required for a signal

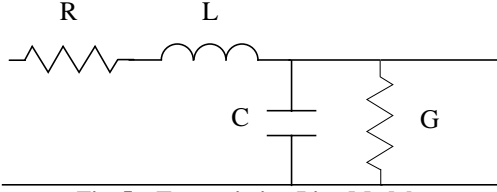


Fig. 5. Transmission Line Model

to move from 10 to 90 percent of its final value. Transmission line effects are prominent when [17]:

$$T_R < 2.5 \cdot T_{FL} = 2.5 \frac{\sqrt{\epsilon_r} R}{c_o} \times l \quad (1)$$

where  $\epsilon_r$  is the relative permittivity of the dielectric,  $l$  is the length of the wire, and  $c_o$  is the speed of light in vacuum ( $\sim 30$  cm/nS). Given 100pS rise/fall times, transmission line effects are significant for lengths exceeding 6.4 mm. For our application, preliminary routing studies suggest trace lengths will approach or exceed this length, warranting further study of transmission line behavior.

A uniform, lossless transmission line can be modeled as having an effective impedance  $Z_0$ . The impedance can be related to the line's electrical parameters [17]:

$$Z_0 = \sqrt{\left(\frac{L}{C}\right)} \quad (2)$$

where  $L$  and  $C$  are the inductance and capacitance of the line. Discontinuities in impedance cause reflections which distort data waveforms. Sources of discontinuities include:

- *changes in characteristic impedance brought about by vias and variations in trace height and width,*
- *the load impedance at the receiving end of the transmission line,*
- *the finite output resistance of the driver.*

We can define reflection ( $\Gamma$ ) and transmission ( $\Gamma+1$ ) coefficients to relate the magnitude of the reflected ( $V_R$ ) and transmitted ( $V_T$ ) waves to the ratio of the impedances forming the discontinuity and the incident wave ( $V_I$ ). The scenario is illustrated in Fig. 6. The fact that the reflected and trans-

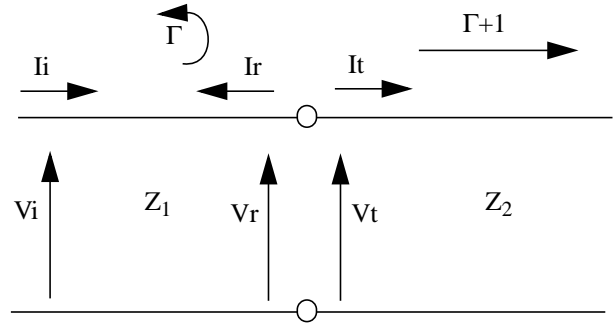


Fig. 6. Discontinuity in a Transmission Line

mitted waves must conform to Ohm's law gives rise to the following expressions:

$$V_R = V_I \left( \frac{Z_2 - Z_1}{Z_2 + Z_1} \right) = \Gamma \cdot V_I \quad (3)$$

$$V_T = V_I \left( \frac{2Z_2}{Z_2 + Z_1} \right) = (\Gamma + 1) \cdot V_I \quad (4)$$

These expressions form the basis for transmission line analysis and can be used to understand reflection noise and the various mechanisms employed to minimize such noise.

For example, if  $Z_2$  is open circuited (the unterminated case),  $\Gamma=1$  and wave is fully reflected. If the line is short circuited, the wave is reflected but changes polarity. If  $Z_2=Z_1$ , there is no reflection and the line is said to be terminated. It is therefore desirable to terminate transmission lines with impedances equal to  $Z_0$ . Termination strategies will be described in Section 4.

### 3.1.2 Self-Induced Noise

The trend toward large, fast ICs has led to both an increase in both average and peak current. Both the power and ground planes have finite inductances (shown in Fig. 1). These inductances are due in large part to the package parasitics (i.e. wire-bond inductance) associated with delivering power to the IC. The I/O driver also sees the inductance at its output. The combination of parasitic inductance and fast current transitions leads to self-induced or switching noise:

$$V = L \frac{dI}{dt} \quad (5)$$

When a large number of drivers are switching in the same direction, the inductance of the power/ground planes will lower/raise the transmitter power supplies relative to the receiver power supplies. A data bit which is in the low state will appear to have a rise in voltage, and the fall time of the drivers will be increased since the on-chip logic low voltage is rising. Rise and fall times will also be degraded due to the signal connector inductance through the same effect. The result is an increase in output delay and overall cycle time.

Bypass capacitors can also be employed to improve power supply stability, however they can cause oscillations by forming a tank circuit with parasitic elements. This is a non-ideal solution.

Another solution is to increase signal transition times (increasing  $dt$  in Eqn. 5). This mitigates the reflection problem for unterminated transmission lines but exacerbates the timing noise problem (as will be shown later). This approach does not solve the problem of self induced noise, but rather accepts the outcome (increased transition times and delay).

Power and ground inductance can be minimized by increasing the number of distribution points and by using low inductance connectors (i.e., flip-chip bumps). This can reduce inductance by an order of magnitude or more. Reducing the currents employed in the signalling system simultaneously reduces power consumption, self-induced noise and system cost.

### 3.1.3 External Power-Supply Noise

Power supply noise can also come from other, uncontrolled sources. The power supply may be susceptible to surges, leading to noise or it may oscillate somewhat due to its internal circuitry and the demands being placed on it (dynamic noise). In battery operated systems, voltages will decay with time (static noise).

### 3.1.4 Coupling Noise

Coupling noise, or crosstalk, is caused by the injection of one signal into another through either parasitic capacitance or inductance. Crosstalk effectively alters signal rise and fall times, adding phase and amplitude noise to the transmitted waveform. Coupling due to parasitic capacitance is of greater significance than inductive coupling because mutual inductances are relatively small. Capacitive coupling can be quantified using Eqn. 6.

$$I = C \frac{dV}{dt} \quad (6)$$

Crosstalk is managed through careful IC, PC board and MCM routing. High-speed signals should be kept apart to minimize coupling effects and signal pins should be interspersed between power pins. Crosstalk can also be reduced by increasing transition times, however, this increases latency and is not the optimal solution.

### 3.1.5 Intersymbol Interference (ISI)

Frequency-dependent attenuation is a major problem at high speeds because it severely reduces signal quality. Reflections occur on a multilevel MCM, even if the lines are perfectly terminated. This is due to package parasitics, vias on the MCM and the fact that MCM signal planes do not always have the same characteristic impedance. A reflection's low frequency signal components are typically attenuated less than its higher frequency counterparts, leading to a phenomena known as intersymbol interference [18]. Low frequency attenuation is caused by the DC resistance of the MCM trace. High frequency attenuation is dominated by the skin effect, but is also caused by the low-pass filter behavior of package parasitics and dielectric loss.

### 3.1.6 IC Processing Noise

Processing variations often occur across a wafer. Variations are expected in  $W$ ,  $L$ ,  $V_t$ , and the

transconductance parameter  $\mu C_o$ . These variations lead to gradient effects both locally and globally.

Global variations occur between chips fabricated on different wafers and to some extent different areas on the same chip. For example, a transmitting chip may have  $n$  and  $p$  transistors with relatively low threshold voltages or shorter than expected gate lengths. This is referred to as a fast/fast process corner. The receiving chip may have been fabricated on another wafer run at a different time, leading to several problems.

A common situation is illustrated in Fig. 7. Often a receiving chip will generate a local reference that it compares to the transmitted waveforms. Threshold variations will alter this reference, creating a DC offset to the receiver. This will lead to unreliable operation and duty-cycle distortion. A solution to this particular problem is to generate the reference at the transmitter and send it to the receiver with the data. In general, the problem of global variation is solved by simulating circuits under ‘worst-case’ conditions, while ensuring proper functionality over all process corners.

Local variations affect the same parameters as global ones, however, they occur in a much smaller area (i.e., between two adjacent transistors). Local variations create DC offsets and AC gain errors in circuits that require precise transistor matching. These offsets must be accounted for in the noise budget along with other more intuitive noise sources.

A typical example involves threshold mismatch in the input transistors of a differential pair (Fig. 8

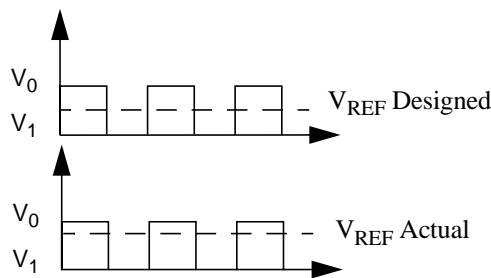


Fig. 7. The effect of processing variations between a transmitter and receiver

(a)). A threshold mismatch between  $M3$  and  $M4$  causes the currents to be unbalanced leading to a DC offset. A threshold shift in  $M5$  leads to an AC gain error by altering the current through the input devices.

Layout techniques are commonly applied to reduce the effects of local process gradients and ensure that circuits operate as desired. The following layout guidelines are applicable to I/O layout:

1. If two transistors have to be matched, they are interdigitized [19]. The practice of interdigitizing transistors reduces the process gradient effect and provides a manageable layout.
2. Large transistors are split into smaller, parallel transistors. This reduces parasitic source capacitance by a factor 2 and parasitic drain capacitance by  $\frac{n+2}{2n}$ , where  $n$  is the number of parallel transistors [20].
3. All transistors have the same orientation.
4. Split transistors are divided into even parts: half with the drain on the left side and the rest with the drain on the right. This is done so that parasitic source and drain capacitances are balanced.

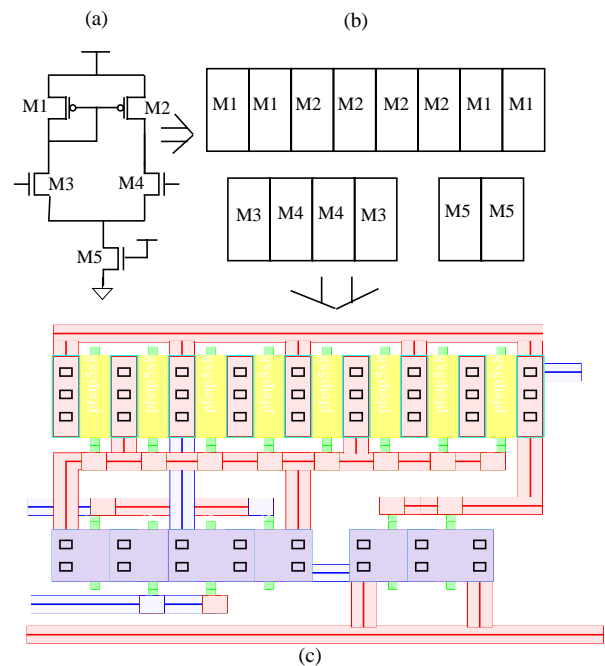


Fig. 8. Differential Pair: (a) schematic, (b) unit cell mapping, (c) final layout

- High speed signals are routed in upper level metals which have the lowest resistance.

Fig. 8 illustrates how a layout is generated. The circuit is first mapped into a suitable interdigitized form. The guidelines given above are then applied, ensuring that the symmetries which exist in the circuit are respected.

### 3.1.7 Summary of Noise

The reliability of a digital interface depends on its ability to cope with noise. The trend towards lower supply voltages and higher clock frequencies is making this a difficult challenge.

It is important to note that coupling, attenuation and power-supply noise are signal dependent. This fact has long been ignored by digital system designers, despite the fact that it leads to the possibility for clever innovation. Instead, the tendency has been to overpower noise, which often creates more noise (i.e. switching noise associated with larger swings).

The study of noise sources leads to several important conclusions regarding high speed digital system design:

- termination should be used to reduce reflection noise,*
- vias and bends in traces should be avoided,*
- low currents combined with advanced packaging approaches are good solutions to the switching noise problem,*
- transition times should be increased as far as the timing and latency requirements will allow,*
- bypass capacitors are helpful and should be incorporated at both the system and chip level,*
- transceiver circuits should have good power supply rejection capabilities,*
- high speed signals should be carefully routed to reduce capacitive coupling,*
- frequency dependent attenuation may be an important consideration, depending on the application,*

- a strict simulation and layout methodology is required to ensure that circuits are reliable and perform as expected.*

## 4. TRANSCEIVER DESIGNS AND TERMINATION SCHEMES

The design of I/O transceivers has become a very active area of research for reasons previously discussed. Emphasis is being placed on reducing power dissipation and improving noise performance. The following sections analyze several transceiver circuits and termination schemes.

### 4.1 LARGE BUFFER

In the 3-4  $\mu\text{m}$  CMOS generation, a large buffer was often used to drive an off-chip load (Fig. 9). This approach is referred to as ‘CMOS signalling’ because full voltage swings are employed. The rise/fall times were high enough that traces could be driven as large capacitive loads. The main advantage to the approach is the simplicity. Disadvantages include:

- the shape factor ( $W/L$ ) of the driver must be several thousand to lower the resistance of the output driver,*
- large output devices occupy a large die area, and are difficult to drive, requiring large and slow pre-driver stages,*
- large transient currents on the power and ground leads of the die make the self-induced power supply noise severe,*

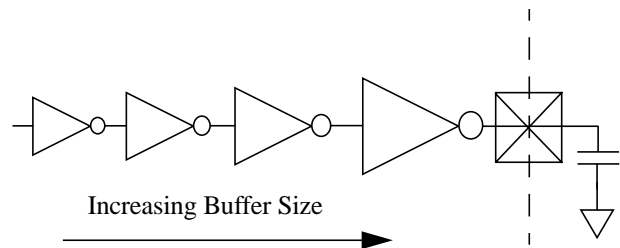
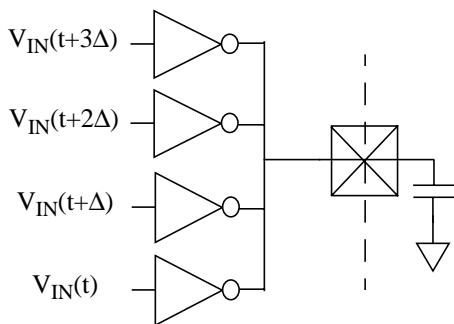


Fig. 9. ‘CMOS’ Signalling



**Fig. 10. Controlled Slew Rate Driver**

- the dynamic power,  $P = CV^2f$ , exceeds 100mW for a typical capacitance of 100pF and modest cycle time of 100 MHz.

#### 4.2 DELAYED RISE/FALL DRIVERS

As technology scaled, the rise and fall times got small enough that transmission line effects became prominent. System designers observed that these effects degraded system performance and adopted a solution whereby signal transition times were increased. A common implementation is illustrated in Fig. 10. A large driver is broken into several smaller ones, each being driven by a delayed version of the input.

This approach reduces reflections by increasing the rise time. It also reduces crosstalk, self-induced  $dI/dt$  noise, and dynamic power dissipation. The shape factor and die area are still high, however. Slowing transitions can be very helpful, but high-performance systems cannot tolerate the increase in latency and phase noise associated with increased transition times.

#### 4.3 SERIES TERMINATION

A driver can be series terminated by matching its output resistance to the characteristic impedance of the line. This relies on the properties of transmission lines for proper operation.

The termination resistance and the characteristic impedance form a voltage divider, and the voltage waveform on the line is a forward propagating step

of amplitude half the driver swing. The receiver has infinite input impedance (i.e. the gate of a MOS transistor), and the reflection coefficient is +1. Therefore, the wave fully reflects, forming a backward wave of half amplitude, that's travels back toward the driver. The superposition of the forward and backward waves at the unterminated end of the line provides a full-amplitude logic swing at that point. The backward propagating wave is fully absorbed as it reaches the driver.

The major advantage of this scheme is that power is dissipated in the termination resistors only during the round trip delay of the line. There are several major drawbacks:

- the design does not employ first-incident wave switching; the transmission time is twice the time-of-flight delay,
- the use of transmission line reflections leads to severe intersymbol interference; residual energy remains on the line and causes hysteresis,
- achieving 50  $\Omega$  driver output resistance requires an enormous driver ( $W/L=1000$  is not atypical).

A solution to the area problem is to use underdamped termination. This is similar in nature to source termination, but the source resistance is larger than  $Z_0$ , producing a damped staircase-like waveform. Underdamped termination still suffers from the other important drawbacks to source termination.

#### 4.4 PARALLEL TERMINATION

An effective way to terminate a transmission line is to place a resistor in parallel with the receiver such that the equivalent resistance seen at the source is matched to the transmission line.

In CMOS systems, the receiver typically has very high input impedance; therefore,  $R_T$  matches the characteristic impedance. A popular circuit is the open-drain circuit shown in Fig. 11 [17]. Volt-

age swings are typically rail-to-rail for the system illustrated.

The termination can be an on- or off-chip resistor, however, it is desirable to use MOS transistors. Processing variations can be overcome by using the automatic impedance control technique [8]. This technique replaces the termination resistor with several parallel MOS transistors. Start-up circuits measure the impedance level and calibrate the termination resistance using registers and look-up tables.

The drawbacks to the open-drain design stem from the large swings employed:

- *large voltage swings that translate to currents on the order of 66 mA for a typical 3.3V supply, leading to severe self-induced noise,*
- *high static power.*

#### 4.5 GUNNING TRANSCEIVER LOGIC

Gunning transceiver logic [21] is an extremely popular signalling scheme. The driver is open drain, but it is sized such that the voltage swings are 0.8V, greatly reducing dynamic power dissipation and noise generation relative to a rail-to-rail circuit. The receiver is a complementary differential pair, with one of the inputs tied to a reference voltage. The scheme is illustrated in Fig. 12.

Reference generation is a major issue surrounding GTL. The reference should be generated at the transmitter side for process tolerance and minimal duty cycle distortion. This makes noise at the transmitter common-mode to the data.

The major drawback to GTL is the static power dissipation associated with the parallel termination scheme. The current swings are much smaller than

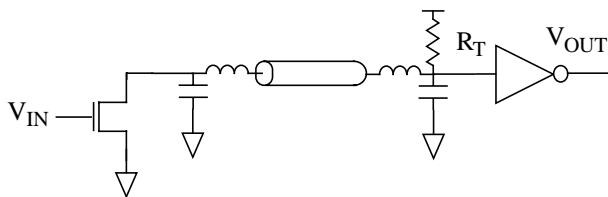


Fig. 11. Open-drain circuit with parallel termination

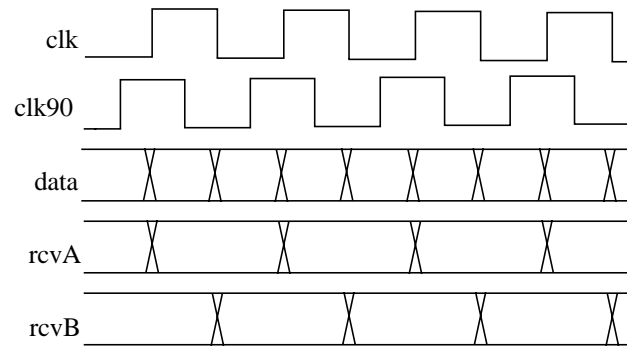


Fig. 13. RAMBUS Timing

the full-swing scheme, but even at 16 mA they cause significant static power dissipation..

The RAMBUS channel [22],[23] is based on GTL. The scheme is illustrated in Fig. 13 [23]. The clock is transmitted in parallel with the data stream. This reduces skew between clock and data. Both clock and data must be routed such that the line lengths are equal. The receiver uses a delay-locked-loop (DLL) to position the sampling clock edge 90° out of phase with the incoming clock. This places the sampling edge in the center of the eye of the receiver, maximizing setup and hold times and reducing the bit error rate (BER). Data is sampled on both edges of the clock. Several variants on this scheme have been proposed [24]-[27]..

#### 4.6 DIFFERENTIAL SIGNALLING

Binary signals can be sent differentially over a pair of traces by driving one trace with a signal and the other with the traces complement. Differential signalling requires twice as many I/O pins as single-ended schemes but has several advantages:

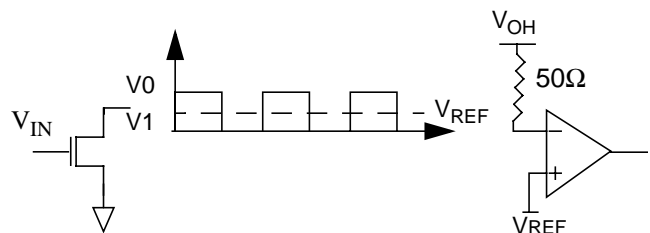


Fig. 12. Gunning Transceiver Logic (GTL)

- the difference in relative voltage swing is twice the single-ended signalling value.
- there is low self-induced power supply noise.

The major drawbacks to this scheme include high static power dissipation and layout area (exacerbated by the pin requirements), and increased routing congestion.

#### 4.7 DYNAMIC TERMINATION

Reducing the static power associated with parallel terminated transmission lines is an important area of research. This section will discuss two approaches to the problem.

The first approach, proposed by Kawahara [28], uses a transmission line that is terminated only during signal transitions. This is accomplished using a standard RC differentiator. The circuit is shown in Fig. 14.

The circuit consists of termination resistors  $RT1$  and  $RT2$ , switching transistors  $M1$  and  $M2$ , and RC differentiators. The sum of the channel resistance of  $M1/M2$  and the termination resistance  $RT1/RT2$  must match the transmission line.

Prior to transition, the transistors are not conducting. During a high to low transition, the voltage at  $N1$  decreases due to capacitive coupling to the input. When the voltage drops below the threshold voltage of  $M1$  it begins to conduct. When  $M1$

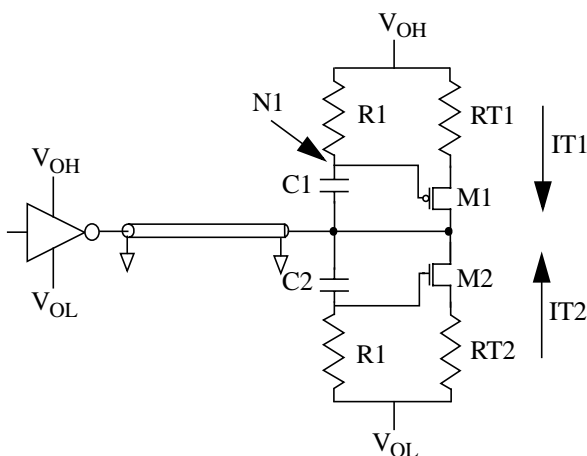


Fig. 14. RC -Based Dynamic Termination Circuit

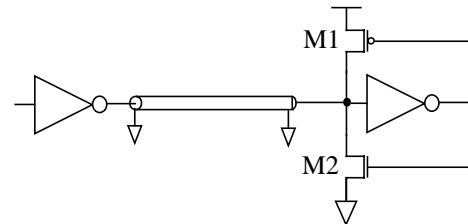


Fig. 15. MOS-Based Dynamic Termination Circuit

reaches saturation the line is terminated by the channel resistance and  $RT1$ .  $N1$  then charges back up according to the time constant formed by the differentiator.

This is a very interesting idea, however several problems surround the implementation. The time constant should be chosen around  $0.1/f$  where  $f$  is the cycle time [28]. In [28],  $0.5 \text{ pF}$  capacitors are used with  $1\text{k}\Omega$  resistors. These capacitors requires a large die area. Other disadvantages include:

- processing variations in the resistor and capacitor make tight control of the RC product impossible,
- the switching transistors must be very large in order to have sub- $50\Omega$  resistance (i.e.  $500/0.3$  for a  $0.3\mu\text{m}$  CMOS process [28]),
- the termination is imperfect for the amount of time required for the RC network to charge/discharge and for the switching transistor to enter saturation; large over/undershoots are observed,
- The solution does not address the self-induced noise problem ( $dI/dt$  is large).

The second dynamic termination circuit [29] uses MOS devices in a latch configuration to terminate the line during transitions. The circuit is shown in Fig. 15.

Transistors  $M1$  and  $M2$  act as termination resistors, again implying large devices. The inverter provides feedback to these transistors to control the termination. Thus, the circuit behaves like a latch. The disadvantages of this circuit are similar to those of the previous one: large die area, severe self-induced noise, and sensitivity to processing variations.

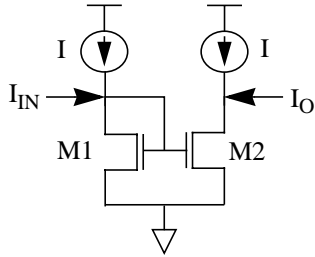


Fig. 16. Linear MOS Current Amplifier

#### 4.8 SWITCHED-CURRENT (SI) DESIGNS

Switched-current (often called current-mode) techniques involve using current signals with little change in voltage. Switched-current (SI) receivers have extremely low input resistance, resulting in inherently low RC delays [34]. The low voltage swings further reduce delay in SI circuits. SI circuits are gaining popularity in low voltage signal processing and A/D conversion because stray-inductance effects are less severe in SI designs than are stray-capacitive effects in SC designs. SI circuits are excellent candidates for I/O design.

A basic element of SI design is the simple current mirror shown in Fig. 16. The diode connected transistor is biased by  $I$ , and operates with a signal current  $i$ , with peak value  $i < I$  to avoid cutoff. This device performs current-to-voltage conversion on its drain current resulting in

$$V_{gs} = \sqrt{\frac{2(I+i)}{k' \left(\frac{W}{L}\right)}} + V_t, \quad (7)$$

thereby performing non-linear I-V conversion. Applying  $V_{gs}$  to the gate of M2, gives

$$I_{ds} = \frac{k'}{2} \left(\frac{W}{L}\right) (V_{gs} - V_t)^2; \quad (8)$$

the inverse of Eqn. 7. Therefore, the resulting output current is a linear function of the input current (related by the W/L ratios of M2 to M1). The input resistance of the circuit is  $\frac{1}{g_m}$ . Channel length modulation leads to undesired mismatch in the gain term.

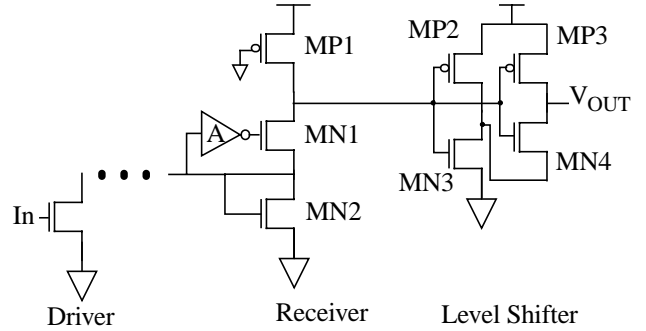


Fig. 17. A Current Mode Transceiver

##### 4.8.1 Cascode Circuit

Steve Long proposed the current-mode circuit shown in Fig. 17 [35]. The circuit is a novel application of a gain-booster cascode circuit [36]. The input resistance of the receiver is approximated as:

$$R_{in} = \frac{1}{(A+1)g_m} \quad t > \tau \quad (9)$$

$$= \frac{1}{g_m} \quad t < \tau \quad (10)$$

where  $g_m$  is the transconductance of MN1 and  $\tau$  is the feedback time of the amplifier. This provides a mechanism for achieving termination. The feedback amplifier is implemented as an inverter with a gain of 22; therefore by biasing MN1 to have  $g_m = 0.9$  mS,  $50\Omega$  termination is achieved. MN2 provides a current reference against which the input current is compared, and MP1 is a load device.

With a 3.3 V power supply, and 0.55V n-thresholds, the output of the receiver can swing from approximately 3.3 to 1.5V. A level shifter is required to convert this voltage to normal CMOS levels. The voltage required by the circuit is 1.5V, making the circuit unsuitable for low voltage applications.

Noise immunity is not effectively addressed by this design. The input impedance is dependent on the gain of the feedback amplifier; a simple inverter is a poor choice in terms of power supply rejection and processing sensitivity.

In [37], the claim was made that the feedback loop will compensate for processing variations. To verify the validity of this claim we must examine the product term,  $Ag_m$ . The gain of the amplifier is given by:

$$A_v = \frac{\sqrt{2}}{\sqrt{I_{AMP}}} \cdot \left( \frac{\sqrt{\beta_n} + \sqrt{\beta_p}}{\lambda_n + \lambda_p} \right) = \frac{C_{AMP}}{\sqrt{I_{AMP}}} \quad (11)$$

where  $I_{AMP}$  is the inverter bias current and  $C_{AMP}$  is a constant. The transconductance of the input transistor is given by:

$$g_m = \sqrt{2} \cdot \sqrt{\beta} \cdot \sqrt{I_{BIAS}} = \sqrt{I_{BIAS}} \cdot C_{BIAS} \quad (12)$$

where  $I_{BIAS}$  is the bias current through MN1 and  $C_{BIAS}$  is a constant related to transistor parameters. The product term becomes:

$$Ag_m = \frac{C_{BIAS} \cdot C_{AMP} \sqrt{I_{BIAS}}}{\sqrt{I_{AMP}}} \quad (13)$$

Let us assume that a global processing variation has lowered the threshold voltages and that both currents have increased by 10%. If  $I_{BIAS}$  is equal to  $I_{AMP}$ , there is no change in the input impedance. However, if  $I_{BIAS} = nI_{AMP}$ , the change can be significant. In [35],  $I_{BIAS}$  was approximately  $37I_{AMP}$ . This would result in a factor of 6 decrease in the  $Ag_m$  term, an intolerable change. Therefore, exclusive reliance on the feedback loop is not enough to ensure process tolerance. The situation could be improved if there were a mechanism in the circuit to maintain a constant ratio of  $I_{BIAS}$  to  $I_{AMP}$ . Unfortunately, the topology of the amplifier and receiver circuits do not lend themselves to this.

The effects of capacitive coupling between data lines is another drawback with this approach. The amplifier input is on the order of 20mV. Therefore, any coupling will seriously distort the amplifier output, making proper reception difficult, if not impossible.

#### 4.8.2 Active Current Mirror Termination

Active current mirrors were first proposed by C.A.T. Salama [38]. Originally, the circuit found application in an algorithmic A/D converter. To

achieve good resolution, a current mirror must display excellent current matching, implying devices that display high output resistance and good parametric matching. Salama observed that by replacing the diode connection in Fig. 16 with an amplifier, the input impedance of the mirror would be reduced by the gain of the amplifier. This led to a reduction in current mismatch equal to the amplifier gain. The amplifier was implemented as a simple differential pair with a gain of 100V/V.

This circuit shows considerable promise as a receiver. The expressions for input impedance are the same as those of the cascode circuit. The circuit retains the desirable properties of the cascode-style circuit, yet is more suitable for low voltage operation.

A proposed implementation is shown in Fig. 19. The behavior of the  $Ag_m$  term is similar to that of the cascode circuit:

$$Ag_m = C \cdot \frac{\sqrt{I_{BIAS}}}{\sqrt{I_{AMP}}} \quad (14)$$

However the use of two bias voltages ( $V_{BP}$  and  $V_{BN}$ ) allows the opportunity for greater process tolerance. This is because the bias current is set by  $V_{BP}$ , while the amplifier current is determined by  $V_{BN}$ . It should be possible to use power supply tolerant biasing techniques to ensure that the ratio  $I_{BIAS}/I_{AMP}$  is constant independent of processing variations.

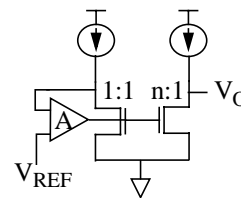


Fig. 18. Active Current Mirror

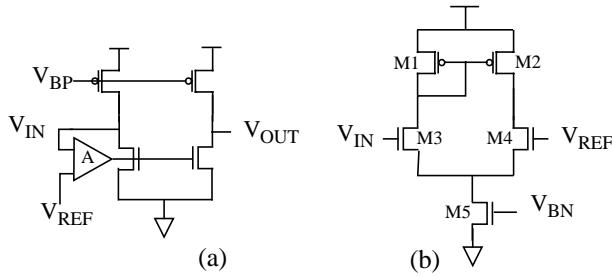


Fig. 19. (a) Proposed Receiver (b) Proposed Amplifier

Finally, the coupling problem is improved by the use of the differential amplifier. The reference voltage,  $V_{REF}$ , will be generated at the transmitter. Therefore, some of the noise will be coupled to both the reference and the data. This noise will be common-mode to both inputs of the differential pair, and will be rejected by the amplifier. The differential amplifier also offers much better power-supply noise rejection than a simple inverter.

The proposed circuit operates at a low supply voltage and offers greater noise immunity than the one proposed in [35]. Successful demonstration of this circuit will likely lead to greater acceptance of switched-current transceiver designs.

## 5. CLOCK RECOVERY ISSUES

Clock extraction circuits are often used in receivers to provide a clock for optimum sampling of input data, independent of process, temperature and data receiver setup variations. VCO-based phase-locked-loops (PLLs) have been used to mitigate several timing problems [39],[30]. It is becoming increasingly difficult to obtain acceptable power supply-induced jitter-performance from PLLs as voltages drop.

Timing noise is caused by jitter and phase offsets. This noise moves the sampling edge from its desired location, increasing the likelihood of setup/hold time violations. Timing noise is of great concern for systems with sub-nanosecond bit times. Jitter is a random quantity related to inherent noise in transistors and to power supply disturbances.

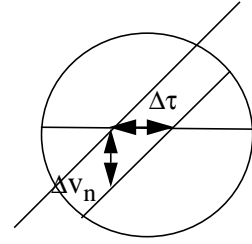


Fig. 20. The first crossing approximation illustrates relationship between timing noise and slew rates.

For I/O design, we do not have to generate a clock, but rather place edges. Thus, there is no need for a VCO, the largest contributor to phase noise. The VCO in PLLs can be replaced by a voltage controlled delay line (VCDL), improving jitter performance substantially [40].

High slew rates make the effect of voltage noise ( $\Delta v_n$ ) have a greater affect on timing ( $\Delta\tau$ ) noise. The first crossing approximation (Fig. 20) illustrates how voltage noise leads to jitter in signals with finite transition times. It is desirable to have sharp clock edges on the MCM/PCB, and a low jitter DLL.

## 6. DELAY-LOCKED-LOOP (DLL) DESIGN ISSUES

A typical DLL block diagram is shown in Figure 25. The phase detector measures the difference between the phase of  $V_{IN}$  and  $V_{OUT}$  and outputs signals that control the charge pump. The charge pump then adds or removes charge from the loop filter, changing the DC value at the input of the bias network. The loop filter stabilizes the loop and filters out high frequency signals. The output of the

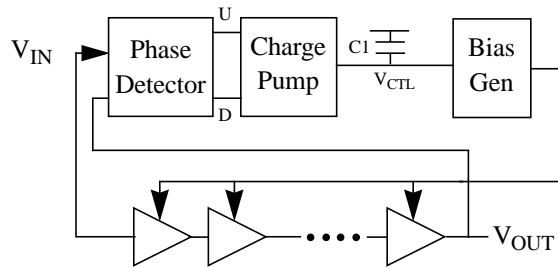


Fig. 21. Single Loop DLL Block Diagram [43]

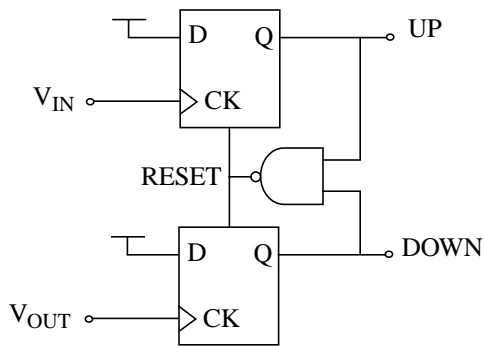


Fig. 22. Typical PD Implementation

bias generator (or sometimes the loop filter itself) controls the VCDL.

The VCDL delays the periodic input by an integer multiple of the period, with zero phase shift. The lowest reported single-loop DLL jitter is 140 pS [40], a significant portion of a sub-nanosecond bit time. The following sections describe the details of low-jitter DLL design.

### 6.1 PHASE DETECTOR DESIGN

Phase detectors are typically implemented using sequential digital logic. Reasons for this include extended tracking range, and low cost [41]. A basic implementation is illustrated in Fig. 22.

The circuit consists of two resettable edge-triggered D-flipflops whose D inputs are connected to a logical ONE. Signals  $V_{IN}$  and  $V_{OUT}$  act as clock inputs to the flipflops. As the phase difference between the inputs decreases, the pulse width on UP or DOWN also decreases. A minimum pulse circuit ensures that the phase detector responds to very small phase differences.

### 6.2 DELAY ELEMENT DESIGN

Delay lines are typically implemented using current starved elements. This means that frequency is controlled by modifying the amount of current available for charging and discharging capacitances.

Differential elements are typically used because they provide good common mode rejection. To

achieve high power supply noise rejection, load elements should have linear I-V characteristics. Dynamic variations in the supply voltage of the buffer stages will cause disturbances in the common-mode buffer output voltages due to parasitic coupling. The resistance provided by MOS loads varies with common-mode voltage and is therefore non-linear. Non-linear load resistances convert common-mode noise into differential-mode noise, affecting the buffer delay.

Linear I-V characteristics provide differential-mode resistance that is independent of the common-mode voltage. Solutions to the linearity problem have been proposed, though suitability for CGaAs has not been studied.

One way to improve the linearity of the load devices is through the use of symmetric impedance loads [43]. A differential circuit with symmetric loads is shown in Fig. 23. Symmetric loads consist of diode connected p-channel devices in parallel with equally sized biased p-channel devices. These loads have the property that their I-V characteristic is symmetric about the point at the center of the voltage swing. It has been shown that these load elements lead to good control over delay and high dynamic power supply noise rejection [43].

### 6.3 BIAS GENERATOR

The buffer stage delay is usually a non-linear function of the applied voltage. This is beneficial because it makes large delay ranges possible. However, as the operating frequency is reduced, the VCDL gain becomes larger, which increases the loop bandwidth relative to the operating frequency.

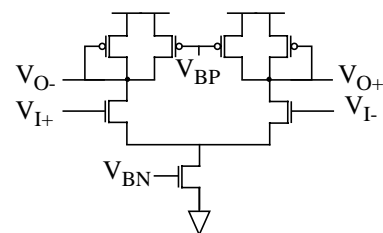


Fig. 23. Differential Delay Stage With Symmetric Loads

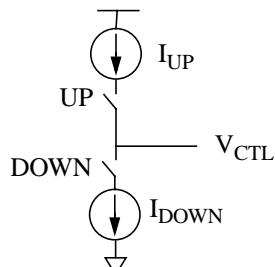


Fig. 24. Simple Charge Pump

This behavior is undesirable because the stability of the loop is undermined at low frequencies, constraining the operating frequency range.

This effect can be corrected by employing self-biasing techniques [43]. This is accomplished using replica circuits in the bias generator. Self-biasing techniques show considerable promise in process and power supply tolerant designs.

#### 6.4 CHARGE PUMP DESIGN

The main issue involved in charge pump design is the desire to have zero charge offset. Small charge offsets lead to significant phase offsets. A conceptual charge pump is shown in Fig. 24. Offsets are caused by parameter mismatch and feedthrough effects on the input switches. The solutions to the feedthrough problem include the use of dummy devices [45], or differential topologies [43].

#### 6.5 DUTY-CYCLE CORRECTOR

Often the duty cycle of the incoming signal is not 50%. This is caused by noise sources such as capacitive coupling and power supply disturbances (i.e. switching noise). The VCDL can further alter the duty cycle, which leads to phase noise. Simple duty-cycle correctors reduce this noise.

#### 6.6 POWER SUPPLY DESIGN

Power supply disturbances are the largest cause of jitter [46]. Power supply noise can be substan-

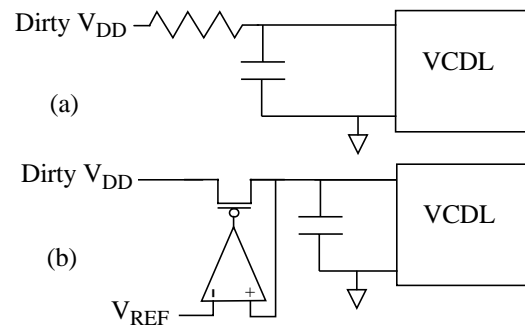


Fig. 25. (a) Supply Filtering (b) Regulation [3]

tially reduced by using filters and regulators local to the VCDL. This is illustrated in Fig. 25. The filter rejects high-frequency (dynamic) noise, while the regulator attempts to maintain a constant DC amplitude. The reference voltage,  $V_{REF}$ , can be generated using a power-supply independent bias generator such as a bandgap reference.

### 7. PROPOSAL

Dr. Richard Wirt, head of Intel's MicroComputer Research Labs, predicts that the current 'system bus' approach to microprocessor design will continue to be employed through 1999. Beyond that, he believes that "a major breakthrough is needed." This breakthrough will likely involve a migration to a point-to-point architecture driven by improved I/O transceivers [47].

I propose to design PUMA's I/O interfaces. The primary goal is to achieve high per-pin bandwidth (2Gb/s/pin) and low latency (< 1 cycle). Other constraints include:

- 4mW maximum power dissipation per link,
- 100mW maximum DLL power dissipation,

The above constraints, along with PUMA's high clock rate, 1.5V power supply, and low threshold voltages, ensure that the proposed solutions will be applicable to future CMOS systems. The following sections describe the required studies.

## 7.1 DATA RECOVERY

The data recovery strategy determines the die area requirements, reliability and power dissipation of a transceiver circuit. Several strategies were discussed in Section 3.1.

The majority of these circuits suffered from some common ailments, caused by large voltage/current swings used to overpower the noise present in the environment. This led to the generation of more noise (dI/dt in particular), high power dissipation and extreme die area requirements. Recent work in the field has focused on reducing the voltage swings required to transmit data (similar to trends in SRAM/DRAM bitline sensing).

Long's approach to the problem demonstrated the feasibility of switched-current techniques. He used feedback to actively terminate a transmission line; the resulting circuitry requires little power and area. However, his work relies on high supply voltages (3.3V), and processing related noise is not addressed.

I propose to modify the active current mirror for use as an I/O circuit. This retains the advantages of Long's approach, is more suitable for low voltage operation, and does not require level shifting circuitry. I plan to improve the noise performance of the circuit by choosing a more suitable amplifier and using special self-biasing [43].

On June 17, 1997, a design was sent to Motorola for fabrication, which included a transmitter and receiver chip for use on a prototype MCM. Also included were structures for characterizing I/O circuits in the presence of controlled noise sources (i.e. ground offsets and dynamic power supply disturbances). The following transceiver designs were implemented:

- *source terminated circuit* [48],
- *delayed transition circuit* [49],
- *open-drain circuit with parallel termination* [17],
- *GTL circuit with parallel termination* [21],

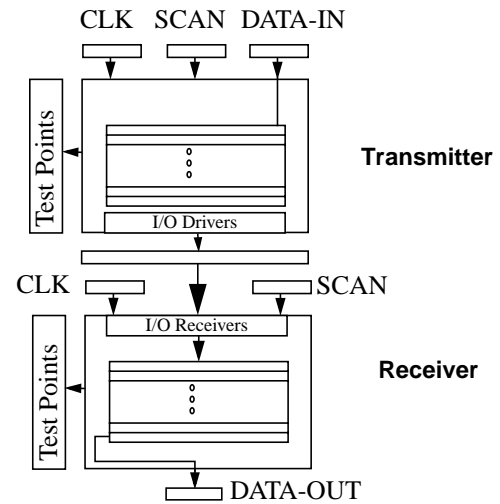


Fig. 26. Transmitter/Receiver Overview

- *UCSB current-mode circuit* [35],
- *active current mirror circuit*.

An overview of the transmitter/receiver chips is shown in Fig. 26. The chips are essentially serial-parallel and parallel-serial converters. This was done to overcome limitations in the testing environment and mitigate the effect of signal-to-signal skews in the probe card and cables.

Each transceiver circuit was carefully sized using a process-tolerant methodology. The methodology ensured that transistors were sized in a near-optimal fashion, assuring the integrity of the study. The circuits were all laid out using the guidelines described in Section 3.1.6.

The results will provide empirical data to support the claims made in section 3.1, and will demonstrate the active current mirror approach. To my knowledge, such a comprehensive study has never been done in one process.

## 7.2 DELAY-LOCKED-LOOP DESIGN

The key to a reliable interface is the design of a low-jitter DLL. Jitter moves the sampling edge away from its desired position, resulting in increased bit error rates. Key issues involved in low jitter DLL design include:

- *buffer stage implementation,*
- *zero-offset charge pump design,*
- *phase detector design,*
- *duty-cycle correction design,*
- *noise rejecting bias circuit design,*
- *regulator design.*

These issues will be addressed and a low-jitter DLL will be designed, fabricated and tested.

### 7.3 CGAAs ESD CIRCUITS

ESD protection circuits significantly increase the parasitic capacitance, creating a trade-off between the level of protection a circuit provides and the speed at which the interface can run.

CGaAs ESD circuits have not been studied as thoroughly as their CMOS counterparts. CGaAs interfaces need tested ESD circuits that give the desired level of protection (and no more).

A test chip has been submitted for fabrication which contains six sizes of two common ESD circuits. The test results will allow me to correlate circuit size and capacitance with protection afforded. Prior to the design of the chip, a sound testing methodology was developed.

#### 7.3.1 Testing Strategy

10-20 chips will be used to evaluate the effectiveness of the ESD protection circuitry. One third of these will act as a control group; they will not be stressed but will be subject to the same handling as the stressed chips. The stressed test chips will be subjected to three positive pulses with one second delay between each and then three negative pulses with a one second delay between each, using an IMCS 5000 ESD tester (available at Motorola's CS-1 facility). The chips will be stressed with voltages ranging from +/-100 V to +/- 10 KV. Failure will be established by analyzing the I-V curve of the input transistor. A damaged gate exhibits a lin-

ear, resistive type of response instead of a normal Ids-Vds curve. The chips will also be inspected using a microscope to observe other types of damage such as damage caused by self-heating in the diodes as well as the input metallization pathways. Time domain reflectometry techniques will be used to determine the capacitance at the input.

## 8. CONTRIBUTIONS TO RESEARCH

My dissertation will advance research in VLSI in the following areas:

- *2 Gb/s/pin interface design issues,*
- *active current mirror termination circuit for low voltage, low power applications,*
- *low-jitter DLL design,*
- *switched-current circuit design,*
- *ESD circuits in CGaAs,*
- *switched-current design issues in CGaAs,*
- *a study of termination circuits for high speed CGaAs interfaces,*
- *low-jitter CGaAs DLL design issues.*

The successful completion of the studies and the ensuing demonstration of a novel switched-current high speed interface encompasses several areas of modern electrical engineering and is extremely relevant to the VLSI community.

## 9. DISSERTATION SCHEDULE

DLL Design	7/97-1/98
Active Current Mirror Study - CMOS	8/97-2/98
Termination study testing - CGaAs	3/98
Test ESD Circuits	2/98
Test DLL and Active Current Mirror (CMOS)	3/98
Design and Test CMOS Prototype Interface	4/98
Implement CGaAs Prototype Interface	4/98-5/98
Begin writing dissertation	4/98
Defend	10/98

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