

A Resonant Clock Generator for Single-Phase Adiabatic Systems

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ABSTRACT

Recently discovered high-speed single-phase adiabatic logic families require efficient sinusoidal power-clock generators. In this paper we propose a low-power resonant clock-generator built around a zero-voltage switching push-pull power conversion topology. We describe a novel energy-efficient control circuit for this power converter, based on an asynchronous CMOS state machine. We also describe an integrated sub-micron CMOS implementation of our power converter and control circuits. Simulation results show efficiencies in excess of 90%, even under suboptimal tuning conditions, for frequencies over 200MHz. We have fabricated our clock generator in a $0.5\mu\text{m}$ standard CMOS process. Using an external surface-mount inductor as the resonant element, we have verified the correct operation of the clock generator when driving a single-phase adiabatic 8-bit multiplier.

Categories and Subject Descriptors

B.0 [Hardware]: General

Keywords

Adiabatic logic, Clock generator, CMOS, Low energy, Resonant, Single phase, VLSI, Dynamic circuitry, SCAL, SCAL-D, TSEL.

1. INTRODUCTION

Efficient power-clock generation plays a crucial role in the design of low-energy adiabatic systems. Due to the multi-phase clocking requirements of most adiabatic circuit families [1, 2, 3, 4, 5], a lot of research has been devoted to the design of efficient generators for multiple-phase or ramp-shaped power clocks [6, 7, 8, 9]. The use of multiple power clocks and tuning elements, coupled with unknown and variable package parasitics, data-dependent load capacitances, and unmatched per-phase clock loads, poses serious challenges to the successful design of such systems, however, particularly at high operating frequencies.

Advances in low-energy circuit design have recently led to the discovery of new high-speed adiabatic logic families that operate

with a true single-phase power clock [10, 11, 12, 13]. These adiabatic systems present a large, primarily capacitive load, requiring rail-to-rail power-clock voltage swings at frequencies comparable to conventional logic families. Moreover, for maximum energy efficiency, they require sinusoidal or symmetrical power-clock waveforms. The resulting AC currents are large and symmetric. A compelling approach to the generation of these currents is the use of low-power, resonant LC -based oscillators.

This paper presents an integrated, single-phase resonant clock generator based on a push-pull, zero-voltage switching power topology akin to a Class-E amplifier [9, 14, 15]. This topology is well-suited for driving the large capacitive loads presented by single-phase adiabatic circuitry, as the peak current conducted by the main power switches is much smaller than the peak inductor current. The resulting power switches are thus small, with small conduction losses and small gate-drive dissipation. To generate symmetric sinusoidal waveforms, our single-phase generator relies on a pair of power switches that are regulated by a highly efficient CMOS controller. The low-energy operation of this controller is based on a tunable ring oscillator and a novel asynchronous CMOS state machine. In this paper, we describe the design, operation, and transistor-level implementation of our clock generator. Through simple analysis, we argue that our generator is suitable for large, practical adiabatic designs. In spice simulations with post-layout extracted parasitics, the reactive efficiency of our generator exceeds 90% at frequencies above 200MHz, even under suboptimal tuning conditions. Our clock generator has been fabricated in a $0.5\mu\text{m}$ conventional CMOS process through MOSIS. Chip measurements show its correct operation above 140MHz, while driving an adiabatic load of approximately 60pF.

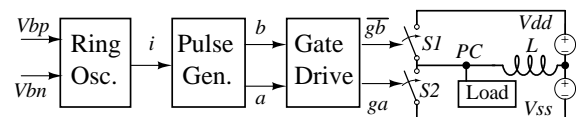


Figure 1: Block Diagram of Clock Generator.

Figure 1 gives a brief overview of our clock generator. Our design is composed of a ring oscillator which feeds a clock signal to a pulse generator. Alternatively, the ring oscillator could be replaced with an external square wave clock source. The pulse generator alternates gate pulses to control the main power switches $S1$ and $S2$. These switches conduct current to and from an external inductor, adding energy to the inductor in a controlled manner from two external DC supplies, which also supply V_{dd} and V_{ss} to the adiabatic circuitry. Switches $S1$ and $S2$ are switched on in an al-

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ternating fashion, pumping the resonant LC system with energy derived from the supplies. This energy is added at the maximum and minimum power-clock voltage, so that the switches are turned on when the blocking voltage is nearly zero. The amount of current conducted by the switches is related to the energy required by the system to maintain a stable power-clock amplitude. For typical adiabatic loads, this current is much less than the peak current flowing through the inductor into the load capacitance.

Previous research in integrated, single-phase clock generators targeted clocked adiabatic circuits [16]. The waveform requirements of these circuits are substantially different from those of the NMOS and PMOS cascades used in recent true single-phase logic families such as TSEL and SCAL [12, 13]. In particular, the use of NMOS and PMOS cascades has eliminated the need for an extra clock signal. Consequently, achieving high energy efficiency requires a more symmetrical power-clock waveform than provided by previous single-phase power-clock generators.

The remainder of this paper has seven sections. Section 2 reviews our selected power conversion topology and its main properties. Section 3 describes the operation of our control circuits. Section 4 gives detailed implementation details, schematics, and simulated waveforms. Section 5 discusses system level considerations, including package parasitics, efficiency, and scaling. In Section 6 we provide simulation results. Section 7 discusses our fabricated clock generator and provides measured operational waveforms. Section 8 summarizes our contribution.

2. OVERVIEW OF POWER TOPOLOGY

In this section we review the properties of the zero-voltage switching resonant power conversion topology we chose for our clock generator. We also justify why this topology is a compelling choice for driving the type of loads we expect from single-phase adiabatic systems.

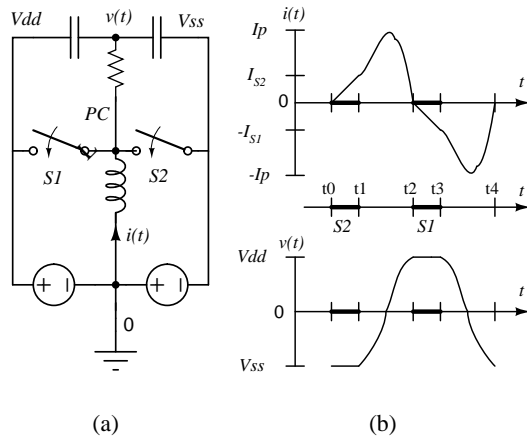


Figure 2: (a) Power conversion topology. (b) Idealized waveforms.

Figure 2(a) presents a switch and resonant element model of our power conversion topology driving a simple resistive and capacitive load. The load is drawn as capacitance to both V_{dd} and V_{ss} to indicate the symmetry of the system. Without loss of generality, however, the following discussion assumes that these capacitances are lumped as a single, equivalent C . The two switches $S1$ and $S2$ are turned on and off in an alternating, periodic manner, so as to pump the resonant LC system at the desired frequency. The in-

ductor L is chosen given a specified C , using the familiar equation $\omega = 1/\sqrt{L \cdot C}$.

Idealized current and voltage waveforms for the inductor and capacitor are shown in Figure 2(b) along with the accompanying switch states. Notice that the peak currents I_{S1} and I_{S2} carried by the switches are smaller than the peak current $\pm I_p$ in the inductor. The switches may conduct current in either direction and can thus transfer any excess resonant energy back into the DC supply. The waveforms drawn assume the duty cycle of the switches is chosen so that in the steady state, the total energy dissipated in the system per cycle exactly balances the energy added per cycle.

An important property of this topology is zero-voltage switching. When $S1$ turns on, the voltage across the switch, V_{ds} , is nearly zero. A similar situation exists for switch $S2$. This zero-voltage switching minimizes turn-on losses associated with the capacitance on the power-clock node.

Another important property of this topology is related to the magnitudes of the currents conducted by the switches. Each switch conducts a current whose magnitude grows in a nearly linear fashion until reaching a peak of I_{Sx} , at which point the switch is turned off. This peak current is related to the energy E_x added to the system by the switch as follows:

$$I_{Sx} = \sqrt{2 \cdot E_x / L} . \quad (1)$$

In steady-state operation, the energy added by the switches exactly balances the losses incurred by the system, and so the peak switch current magnitude is independent of the peak load current. In addition, as we scale the magnitude of the load losses by α , the size of the switches only needs to scale by $\sqrt{\alpha}$, assuming that the current carrying capacity of a MOSFET switch is proportional to its W/L ratio.

Since switch size and conduction losses are proportional to the peak switch current that needs to be conducted, this power topology is very efficient at driving large capacitive loads with low-dissipation. The single-phase adiabatic logic families we have considered present exactly this type of load [12], due, in part, to the large capacitance associated with the power-clock distribution tree. In addition, these families require large resonant power-clock currents, while incurring small losses on the power-clock. This type of load is exactly what can be driven efficiently with the small switches of this topology.

3. OPERATION

In this section, we describe the operation of the circuitry that controls switches $S1$ and $S2$. This circuitry must provide alternating pulses of controlled width to the two switches at a constant rate. The main cost metric is energy dissipation per cycle in the control logic.

As shown in Figure 3, our control circuitry consists of a three-stage differential-logic ring oscillator, a ratioed inverter to generate duty-cycle controlled pulses, and an asynchronous state machine, that alternates the two pulses to the two switches. The ring oscillator is controlled by two bias voltages V_{bn} and V_{bp} . In particular, the overall clock period is controlled by adjusting V_{bn} and V_{bp} in opposite directions. This adjustment increases or decreases the total current available for the differential inverters. The pulse width of the buffered output i is controlled by adjusting V_{bn} and V_{bp} in the same direction. This type of adjustment changes the common-mode level of the differential signals, which gets converted to pulse width variations by the ratioed inverter.

Figure 4 shows the state transition diagram associated with the asynchronous state machine. Other than an initial reset signal, the state machine operates from the single input i , which is derived

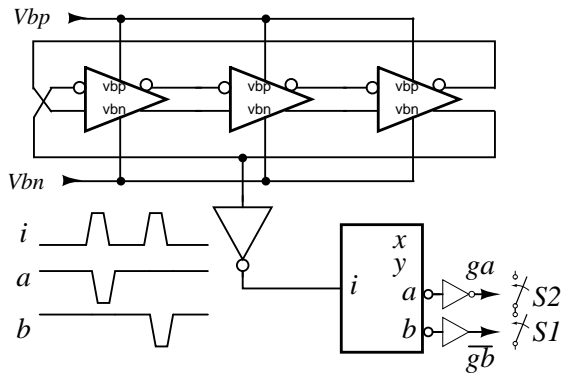


Figure 3: Block diagram of control logic.

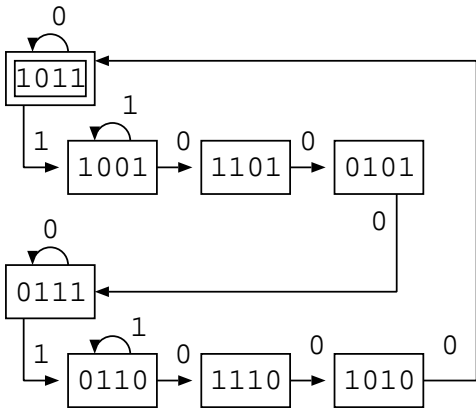


Figure 4: State diagram of pulse generator, with state bits corresponding to nodes x , y , and b .

from the ring oscillator. The function of the state machine is to direct positive-going pulses on i alternately to negative-going pulses on state bits a and b . The widths of the pulses on a and b are proportional to the width of the pulses on i . Furthermore, the states are assigned in such a manner that each state transition amounts to a single bit change. Each positive bit transition is uniquely identified by two “zero” state bits, and each negative bit transition is uniquely identified by two “one” state bits. This specific state encoding leads to a very compact asynchronous CMOS implementation of this state machine, involving 16 transistors and 1 reset transistor. The main timing assumption for this circuit is that the input pulses are long enough for the state machine to reach a stable state before the input changes. Detailed transistor-level schematics for this state machine are provided in Section 4.

4. IMPLEMENTATION

The complete clock generator circuits are shown in Figure 5, targeting a $0.5\mu\text{m}$ standard CMOS process, a frequency of 200MHz, and a driving load of 60pF. The ring oscillator contains 27 transistors, including the output buffer. The sizes of the transistors feeding current into the ring oscillator inverters are chosen to normalize the voltage amplitudes between the two lightly loaded differential inverters and the single, heavily loaded differential inverter that drives the ratioed inverter. The three weak PMOS transistors with a W/L ratio of 3/4 are provided to slightly imbalance the ring oscillator, allowing for more reliable oscillator startup in simulation.

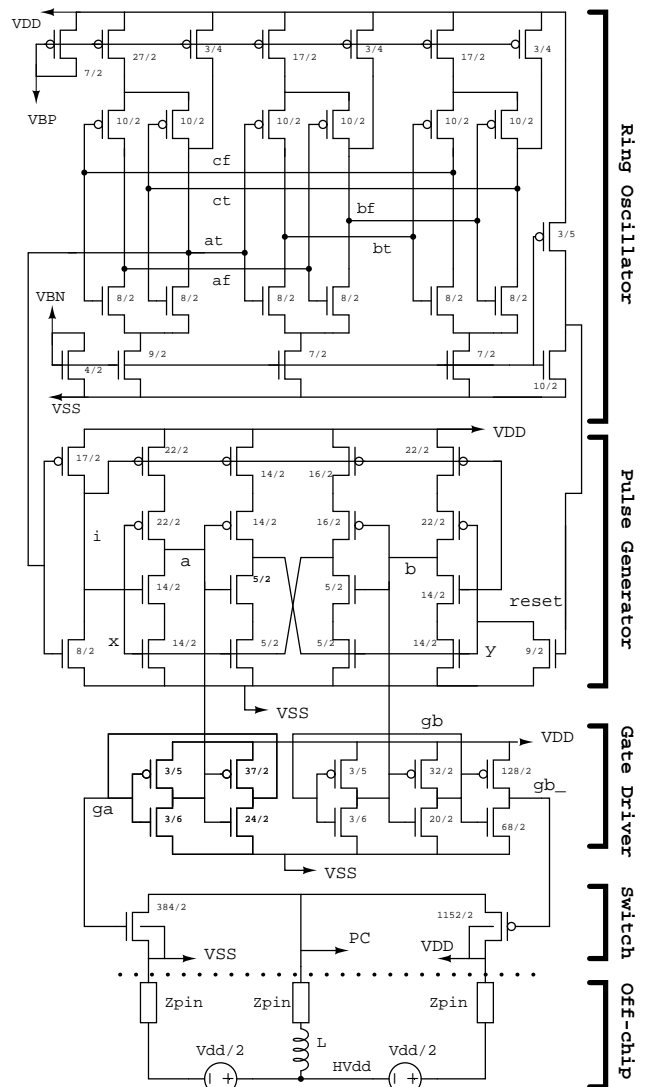


Figure 5: Detailed schematic of clock generator.

An internal reset signal is derived from the V_{bn} bias input.

The pulse generator state machine contains 17 transistors. The two transistor stacks driving the nodes a and b are sized almost twice as large as the stacks driving the nodes x and y . Nodes x and y are fully dynamic, while nodes a and b have weak keeper transistors providing positive feedback current from the gate drive. The gate drive circuits comprise 10 transistors. We provide two inverters to amplify the signal b that drives the main PMOS power switch. We provide one inverter to amplify the signal a that drives the main NMOS power switch. In our layout, the two power switches are segmented into a number of smaller transistors, each of them surrounded by a guard ring and connected with many contacts to reduce the contact resistance. The PMOS power switch is approximately 3 times the size of the NMOS power switch, reflecting the reduced current carrying capability of the PMOS devices in this technology.

Figure 6 shows simulation waveforms from our clock generator, when driving a capacitive load of 60pF with a resonant inductance of 12nH. The top trace shows signals at , bt , and ct from the ring oscillator. The second trace shows the internal signals

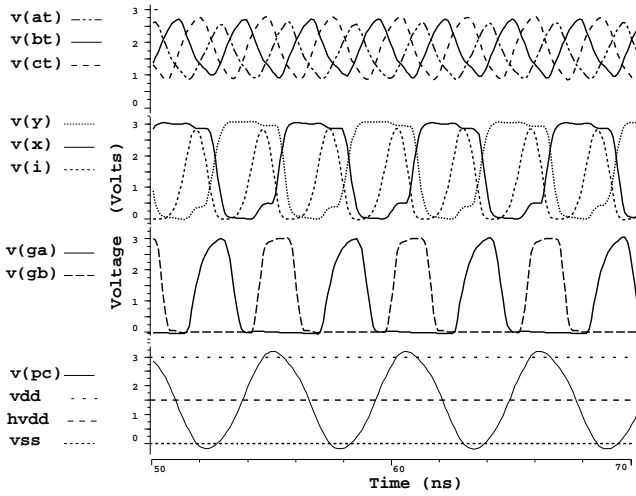


Figure 6: Example clock generator waveforms.

i , x , and y from the clock control state machine. The third trace shows the buffered gate drive pulses ga and gb , which are inverted versions of signals a and b from the clock control state machine. The NMOS power switch is controlled directly by ga . The PMOS power switch is controlled by gb , which is an inverted version of gb . Since the PMOS power switch is roughly 3 times as large as the NMOS power switch, the additional inverter buffering the gate drive also provides additional signal gain. The fourth trace shows the resulting power-clock waveform, along with the three DC supply voltages V_{dd} , V_{ss} , and HV_{dd} as a reference.

5. SYSTEM LEVEL ISSUES

5.1 Adiabatic Load

Single-phase adiabatic logic families require a single power-clock signal to be distributed to each gate in the design, while minimizing the voltage drop and phase shift between any two points on the power-clock grid. The physical design of the power-clock grid usually entails laying out many wide distribution wires, contributing a significant amount of capacitance to the power-clock node, upwards of 60% in the designs we considered. With our power-clock generator, this additional capacitance does not significantly impact overall efficiency, because the main power switches only need to conduct a current sufficient to balance the losses incurred by the load, and not the entire inductor current.

5.2 Efficiency

In order to effectively measure the performance of the clock-generator driving a reactive (primarily capacitive) load, we use a standard definition for efficiency usually applied to AC power systems that includes a measure of reactive energy. This is an appropriate performance metric, because the adiabatic logic families require a large amplitude sinusoidal voltage in order to operate correctly, but dissipate only a small fraction of the energy stored in the resonant elements per cycle. We adopt the usual definition for reactive power, namely the product of RMS voltage and RMS current. Using symbols related to our design, the efficiency equation becomes:

$$\eta = \frac{(v_{load})_{RMS} \cdot (i_{load})_{RMS}}{P_{cg} + (v_{load})_{RMS} \cdot (i_{load})_{RMS}},$$

where P_{cg} is the power dissipated within all of the clock generator

circuits. In the case of a purely resistive load, the reactive power and real power are identical and this equation reduces to the familiar equation

$$\eta = P_{load} / (P_{cg} + P_{load}).$$

5.3 Scaling

We consider the effect of changing the adiabatic load capacitance on the efficiency of our clock generator. Given are two adiabatic loads with identical dissipation E_{load} , differing only in the load capacitance C_1 and C_2 . Assuming we want to compare the performance of our clock generator at the same frequency for these two load capacitances, it is necessary to scale the inductor size as follows:

$$L_2 = L_1 \cdot C_1 / C_2.$$

Since the clock generator losses are proportional to the peak current conducted by the main power switches, comparing the expressions for I_{Sx} indicates how the losses compare between the two designs:

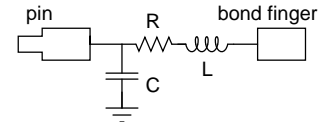
$$I_{Sx,2} / I_{Sx,1} \sim \frac{\sqrt{1/L_2}}{\sqrt{1/L_1}} \sim \sqrt{C_2 / C_1}.$$

Thus, adding pure capacitance to the load increases our clock generator losses by only the square root of the increase in capacitance.

In general, we expect very large loads to be relatively more efficient per computation than small loads. The overhead of supporting a ring oscillator and pulse generator is amortized over all of the load losses. Moreover, the losses associated with the scalable components of the clock generator, namely the power switches and gate drive circuits, grow only in proportion to the load losses, independent of the load capacitance. In particular, given an adiabatic design that occupies area A , both the capacitance and load energy dissipation E_{load} are roughly proportional to A . Also, for fixed frequency, L is inversely proportional to C . Substitution into Equation 1 that gives the peak switch current yields

$$I_{Sx,peak} \sim \sqrt{E_{load} / L} \sim \sqrt{A / (1/A)} \sim A.$$

5.4 Package Parasitics



$$C = 1.05 \text{ pF} \quad L = 3.69 \text{ nH} \\ R = 0.0498 \text{ Ohms}$$

Figure 7: MOSIS 40-pin ceramic DIP package parasitics, pins 8, 13, 28, and 33.

Package parasitics may negatively impact the performance of our clock-generator if not considered in the system level design as they may vary widely between package types and even between pins within the same package. As an example, we provide in Figure 7 the parasitics model for a 40-pin ceramic DIP package used by MOSIS. This was the package selected for our test chip. Using the parasitics information, we chose to use 6 pins near the shortest package leads (pins 8, 9, 10, 11, 12, 13), allocating 2 pins to each of V_{dd} , V_{ss} , and PC . The parasitics for these pins were in the range $L = [3.15 \text{ nH}, 3.69 \text{ nH}]$, $C = [0.660 \text{ pF}, 1.05 \text{ pF}]$, $R = [0.0247 \Omega, 0.0498 \Omega]$. There are many modern packages that have much better characteristics than the 40-pin DIP. Nevertheless,

the package parasitics and pin choices must be carefully considered, because large AC currents are present in the V_{dd} , V_{ss} , and PC nodes of our clock generator, even if the DC component is small.

6. SIMULATION RESULTS

6.1 Equivalent RC Loads

To evaluate the efficiency of our clock generator, we simulated its operation in HSPICE using a lumped RC load, whose values were chosen to be representative of the target adiabatic system. To determine appropriate values for C_{load} , we first measure the RMS current and voltage present at the power-clock input of our adiabatic circuit. We then compute C_{load} using the expression

$$C_{load} = \frac{1}{\omega \sqrt{(V_{RMS}/I_{RMS})^2 - (P_{loss}/I_{RMS}^2)^2}}$$

For most adiabatic circuits, it is reasonable to assume that $R \ll 1/(\omega C)$ which, in which case C_{load} can be approximated by the expression

$$C_{load} = \frac{I_{RMS}}{\omega V_{RMS}}$$

In addition, we measure the total power dissipation of our adiabatic circuit attributed to the power-clock source by integrating the power over one cycle:

$$P_{loss} = \frac{1}{T} \int_0^T v_{pc}(t) i_{pc}(t) \delta t.$$

From this dissipation we pick an equivalent resistance R_{load} using the expression

$$R_{load} = P_{loss}/I_{RMS}^2.$$

The adiabatic circuit we used in our simulations was an 8-bit multiplier [12]. For this circuit, we computed equivalent RC values of approximately 60pF and 0.91Ω. With these equivalent load parameters, the dissipation within the clock generator, P_{cg} , is computed from the voltages and currents present on the V_{dd} and V_{ss} supplies as follows:

$$P_{cg} = \frac{1}{T} \int_0^T (V_{dd} \cdot i(V_{dd}) + V_{ss} \cdot i(V_{ss}) - R_{pc} \cdot i_{pc}^2) dt.$$

6.2 Bias Control

Figure 8 shows a contour plot showing the effect of the ring oscillator bias voltages on frequency and switch duty cycle. The dashed contours indicate frequency and are labeled in units of MHz. The solid contours indicate switch duty cycle in percent, as measured on the gate of the main power switches. This plot shows how to select the correct bias voltages for a given operating condition. It also demonstrates the capability for our control circuits to be tuned.

The two bias voltages can be efficiently generated on-chip using a variety of standard techniques [17]. Since the biases are connected only to polysilicon gate conductors and metal wires, the leakage current is negligible, so the only dissipation would come from the bias generator circuit itself.

6.3 Efficiency and Tuning

Figure 9 shows the effect of tuning mismatch on efficiency. A fixed bias was applied to the ring oscillator, generating a frequency of 207MHz. Different inductances were chosen, so that the resonant frequency varied from the ring oscillator frequency by $\pm 10\%$. This experiment was repeated for several different load configurations, chosen so that the product RC was held constant at

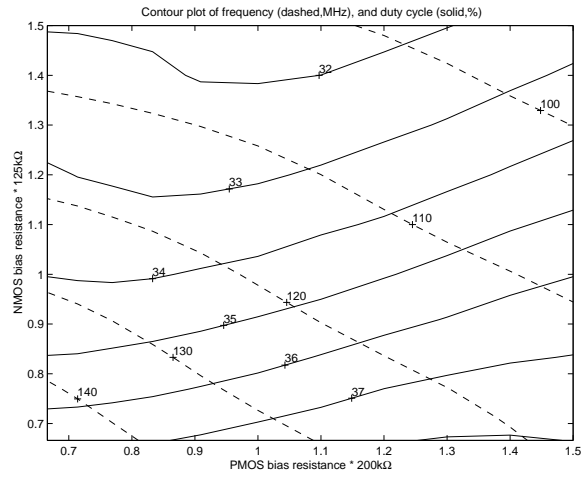


Figure 8: Bias control of frequency and switch duty cycle.

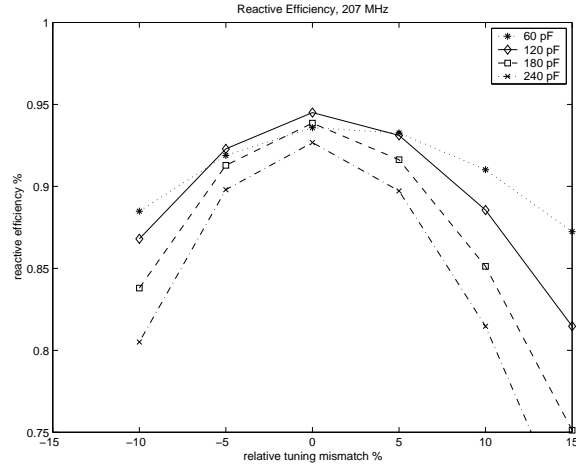


Figure 9: Reactive efficiency vs. inductor mismatch.

$60pF \cdot 1\Omega$, which is a conservative representative of our adiabatic loads. The goal of these simulations was to determine the robustness of the system to real world component and package parasitic variation. As indicated by our data, we expect our clock generator to achieve efficiencies in excess of 90% with an inductor component tolerance of $\pm 5\%$.

7. EXPERIMENTAL RESULTS

Figure 10 shows a close up photograph of the clock generator, which was fabricated as part of a larger single-phase adiabatic logic test chip. The clock generator occupied an area of 0.012 mm^2 and was capable of driving an adiabatic circuit composed of 11,854 transistors occupying an area of 0.710 mm^2 . The area overhead of the clock generator was thus less than 2% of the total design. In comparison, the bypass capacitance required to reduce supply noise for this same design amounted to 6% of the design area.

The clock generator was designed as part of an adiabatic multiplier design project and was thus hardwired to its load. Consequently, clock efficiency could only be indirectly measured by subtracting the dissipation of the multiplier from that of the entire clock and multiplier system. Since the experimental characterization of the multiplier's dissipation had limited accuracy, the error

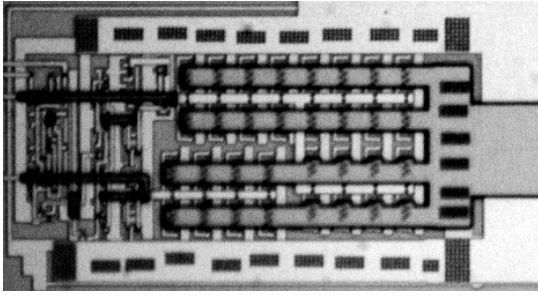


Figure 10: Microphotograph of clock generator.

in multiplier dissipation was of the same order as the clock generator dissipation, rendering the efficiency computation meaningless. However, measurements of total clock and multiplier system dissipation were consistent with our simulations.

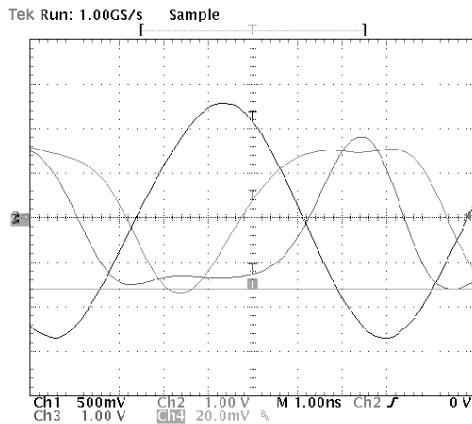


Figure 11: Measured waveforms: power-clock, g_a and g_b - signals.

Figure 11 shows measured waveforms of the clock generator driving an on-chip adiabatic load of approximately 60pF and 0.91 Ω . An external surface-mount inductor was used as the resonant element. The large sinusoid is the power clock signal measured at the external inductor pin. The two smaller waveforms are buffered versions of the gate drive signals g_a and g_b . Due to the delay of buffering and driving external pads, these pulses do not appear on the same phase of the power-clock sinusoid as the internal gate drive signals.

The use of an inductor with a highly integrated CMOS chip presents the possibility of latch-up, as potential voltage overshoots may cause excessive substrate currents triggering latch-up. Throughout the testing of our fabricated chip, we did not experience latch-up under any conditions, even with voltages outside of normal operating conditions. As latch-up was a design concern, we provided a large on-chip bypass capacitor to store any excess energy from the inductor, conducted back into the supplies through the main switches. Moreover, we segmented the main power switches in our layout, separating segments with substrate or well contacts.

8. CONCLUSION

We have presented a compact, tunable, and highly-efficient integrated clock generator circuit, suitable for efficiently driving large capacitive loads such as those presented by recent single-phase adiabatic circuit families. We presented a simple and efficient asyn-

chronous state machine for generating the required alternating gate drive pulses for a push-pull zero-voltage switching power converter. With reactive efficiencies exceeding 90%, we have shown that our clock generator is well-suited for driving the types of loads presented by adiabatic circuit families. We have fabricated and successfully tested the operation of our circuits in a standard 0.5 μm CMOS process.

9. ACKNOWLEDGMENTS

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