

True Single-Phase Adiabatic Circuitry

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Abstract—Dynamic logic families that rely on energy recovery to achieve low energy dissipation control the flow of data through gate cascades using multiphase clocks. Consequently, they typically use multiple clock generators and can exhibit increased energy consumption on their clock distribution networks. Moreover, they are not attractive for high-speed design due to their high complexity and clock skew management problems.

In this paper, we present TSEL, the first energy-recovering (a.k.a. adiabatic) logic family that operates with a single-phase sinusoidal clocking scheme. We also present SCAL, a source-coupled variant of TSEL with improved supply voltage scalability and energy efficiency. Optimal performance under any operating conditions is achieved in SCAL using a tunable current source in each gate. TSEL and SCAL outperform previous adiabatic logic families in terms of energy efficiency and operating speed. In layout-based simulations with $0.5\mu\text{m}$ standard CMOS process parameters, 8-bit carry-lookahead adders (CLAs) in TSEL and SCAL function correctly for operating frequencies exceeding 200MHz. In comparison with corresponding CLAs in alternative logic styles that operate at minimum supply voltages, CLAs designed in our single-phase adiabatic logic families are relatively more energy efficient across a broad range of operating frequencies. Specifically, for clock rates ranging from 10MHz to 200MHz, our 8-bit SCAL CLAs are 1.5 to 2.5 times more energy efficient than corresponding adders developed in PAL and 2N2P and 2.0 to 5.0 times less dissipative than their purely combinational or pipelined CMOS counterparts.

Keywords—Energy recovery, adiabatic logic, true single-phase clocking, high performance, low-power design, low power dissipation, dynamic logic.

I. INTRODUCTION

Energy recovery is a promising approach to the design of VLSI circuits with extremely low energy dissipation. Energy-recovering circuits achieve reduced energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads [1], [2], [3], [4], [5]. They are thus often referred to as *adiabatic circuits*, due to the resemblance of their operation to adiabatic state changes in physical systems. In general, adiabatic circuits that operate very efficiently at low operating frequencies stop functioning at high data rates. Conversely, adiabatic circuits that can function correctly across a broad range of operating frequencies tend to be dissipative at low frequencies. These circuit families rely on multiphase clocks to control cascaded gates. They are consequently unattractive for high-speed and low-power system design due to the plethora of design problems associated with multiphase clocking such as increased energy dissipation, layout complexity in clock distribution, clock skew, and multiple power-clock generators.

Various adiabatic circuit families have been proposed over the past few years. They all use at least two power-clock phases to control gate cascades, however. A scheme with asymptotically zero dissipation that requires reversible computations was described in [3]. Several relatively simple adiabatic logic styles that use diodes to avoid reversibility were proposed in [6], [7], [8], [9]. Circuit families that use a pair of cross-coupled transistors to adiabatically charge and discharge their loads were

introduced and evaluated in [10], [11], [12], [13], [14], including 2N2P, 2N-2N2P, pass-transistor adiabatic logic (PAL), and clocked CMOS adiabatic logic (CAL).

This paper presents the first-ever true single-phase adiabatic circuit family that is geared towards high-speed and low-energy VLSI design. The simplest member of our family is TSEL. In TSEL, high speed operation is ensured by non-adiabatically activating a pair of cross-coupled transistors and by adjusting two DC reference voltages. Low energy consumption is achieved by adiabatically charging and discharging capacitive loads through the cross-coupled transistors. TSEL cascades are implemented straightforwardly in an NP-domino style.

The second member of our family is SCAL, an enhancement of TSEL with improved scalability and energy efficiency. SCAL is a source-coupled adiabatic logic that achieves lower energy dissipation than TSEL for a broad range of operating frequencies. SCAL gates are derived from TSEL gates by replacing each DC reference voltage line by a current source. Each current source can be individually tuned by transistor sizing to achieve optimal non-adiabatic charging/discharging rates for its operating conditions. Both TSEL and SCAL gates are dual-rail and always present a balanced load to the clock generator, regardless of the particular data computed. Moreover, they are both functionally complete.

We have designed and simulated in HSPICE a variety of arithmetic circuits, including carry-lookahead adders (CLAs) and Hadamard Transform (HT) modules for wireless communication [15], [16]. This paper describes our findings with a collection of 8-bit CLAs that we designed in TSEL, SCAL, other adiabatic logic styles, and static CMOS. In layout-based simulations with $0.5\mu\text{m}$ standard CMOS process parameters, the 8-bit CLAs in TSEL and SCAL function correctly for operating frequencies exceeding 200MHz with minimum-size transistors used in the evaluation trees of each gate. In comparison with corresponding adders in alternative logic styles and minimum possible supply voltages, TSEL and SCAL are more energy efficient across a broad range of operating frequencies. Specifically, for clock frequencies ranging from 10MHz to 200MHz, our 8-bit SCAL CLAs are 1.5 to 2.5 times more energy efficient than corresponding adders developed in PAL and 2N2P and 2.0 to 5.0 times less dissipative than their purely combinational or pipelined static CMOS counterparts. For clock frequencies ranging from 100MHz to 200MHz, TSEL adders are as energy efficient as their corresponding designs in SCAL.

The remainder of this paper has five sections. In Section II we review the adiabatic logic families most closely related to TSEL and SCAL. The structure and operation of TSEL gates and cascades are described in Section III. The structure and operation of SCAL gates and cascades are presented in Section IV. Our adder designs are described in Section V. Section VI presents simulation results from layouts of our 8-bit carry-lookahead adders that were designed using a $0.5\mu\text{m}$ standard CMOS tech-

nology. Our contributions and ongoing research are summarized in Section VII.

II. OVERVIEW OF ADIABATIC LOGIC FAMILIES

This section highlights the operation of static CMOS and several adiabatic logic families related to TSEL and SCAL. We focus on the characteristics of the adiabatic logic families 2N2P, 2N-2N2P, PAL, and CAL that use a cross-coupled transistor structure for adiabatic operation similar to TSEL and SCAL.

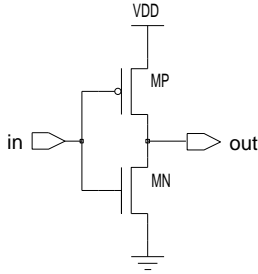


Fig. 1. Static CMOS inverter.

The dominant factor in the dissipation of static CMOS logic is the power required to charge capacitive nodes. In the CMOS inverter of Figure 1, when the power supply drives the output node high, the voltage V_{dd} is applied abruptly resulting in a high voltage drop across the PMOS switching device MP. The total energy drawn from the power supply is $E_c = CV_{dd}^2$, where C is the capacitance of the output node and V_{dd} is the supply voltage. Half of this energy is dissipated on the on-resistance R of the device MP, and the other half is stored in the output capacitance. When the output is driven low at a later cycle, the energy stored in the output capacitor is dissipated on the on-resistance R of the device MN.

In contrast to conventional CMOS circuits, adiabatic circuits charge or discharge capacitors while striving to keep the potential drop across their switching devices small. Thus, only a fraction of the energy supplied during each cycle is dissipated on their resistive components. The bulk of the supplied energy is returned to the power supply and can be reused in subsequent cycles. Typically, power supplies for adiabatic circuits provide a time-varying, periodic output signal, or power-clock, that gradually swings between 0V and V_{dd} . The period of this signal is long enough to maintain a small potential drop V_R . A simple form of adiabatic charging can be accomplished using a power supply with a ramp output. Such a signal can be approximated using a resonant RLC oscillating structure. Other adiabatic generator designs have been presented in [3], [17], [18]. The number of power-clocks required to control cascaded gates is an important consideration in adiabatic logic design, since it affects energy dissipation, operating speed, and design complexity.

Figures 2 and 3 show inverters from 2N2P and 2N-2N2P, two related adiabatic logic families that have no diodes and use four-phase clocks to control cascades [11]. These families exhibit a non-adiabatic dissipation proportional to CV_{tp}^2 , where V_{tp} is the threshold voltage of PMOS devices in a pair of cross-coupled transistors. The non-adiabatic switching event occurs during a brief interval in the beginning of the evaluation phase and provides the voltage differential that activates a cross-coupled tran-

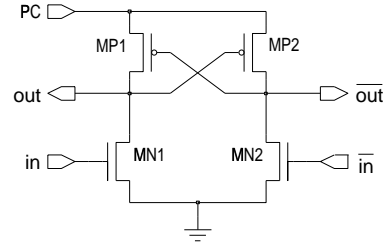


Fig. 2. A 2N2P inverter. Cascades require four power-clock phases in quadrature.

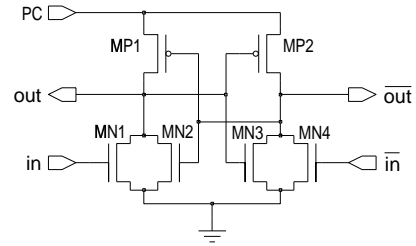


Fig. 3. A 2N-2N2P inverter. Cascades require four power-clock phases in quadrature.

sistor structure similar to the one used in the Sample-Set Differential Logic (SSDL) [19]. 2N2P and 2N-2N2P present a balanced capacitive load and possess superior speed characteristics than other adiabatic families in this section. The primary advantage of 2N-2N2P over 2N2P is that the pair of cross-coupled NMOS switches results in non-floating outputs.

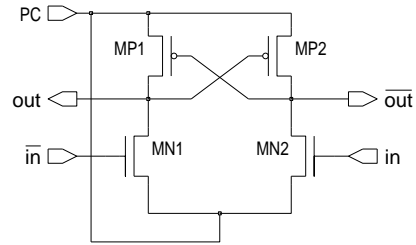


Fig. 4. A PAL inverter. In this logic family, cascades require a two-phase power-clock.

Figure 4 shows an inverter in PAL, an adiabatic logic family similar to 2N2P [13]. In PAL, the ground node of 2N2P is connected to the power supply in order to eliminate non-adiabatic energy consumption. PAL achieves fully adiabatic operation at the cost of high-speed operation. Cascaded PAL gates are controlled by a two-phase clock.

Figure 5 shows an inverter designed in CAL, an adiabatic logic related to 2N-2N2P [14]. The main structural difference between CAL and 2N-2N2P is the path control switches in the pull-down tree. In CAL, cascaded structures are controlled by a single-phase clock and two auxiliary square-wave clocks. Thus, even though this logic is referred to as single-phase, its cascades are controlled by three waveforms. In terms of their operating speed, CAL gates are comparable to 2N-2N2P gates. CAL circuits achieve half the throughput of corresponding 2N-2N2P circuits, however, because they enable logic evaluation in alternate clock cycles. Moreover, CAL designs tend to be more dissipative than 2N-2N2P, due to their higher device count.

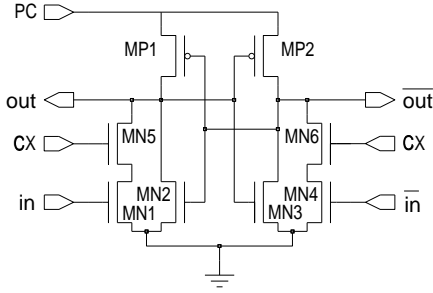


Fig. 5. A CAL inverter. Cascades require a single-phase power-clock and two auxiliary square-wave clocks.

III. TRUE SINGLE-PHASE ENERGY-RECOVERING LOGIC

TSEL is a partially adiabatic circuit family akin to 2N2P, 2N-2N2P, and CAL. Power is supplied to TSEL gates by a single-phase sinusoidal power-clock. Cascades are composed of alternating PMOS and NMOS gates. Two DC reference voltages ensure high-speed and high-efficiency operation. They also enable the cascading of TSEL gates in an NP-domino style. This section describes the structure and operation of TSEL.

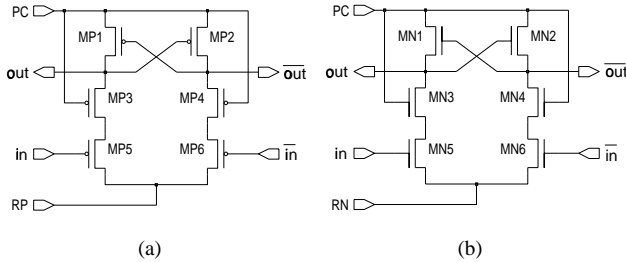


Fig. 6. (a) A PMOS and (b) an NMOS inverter in TSEL.

A. TSEL Gates

The basic structure of a TSEL PMOS gate is shown in the PMOS inverter of Figure 6(a). This inverter comprises a pair of cross-coupled transistors (MP1 and MP2), a pair of current control switches (MP3 and MP4), and two function blocks (MP5 and MP6). The port PC supplies the sinusoidal power-clock V_{PC} . The port RP supplies a constant reference voltage V_{RP} to the PMOS gate. Inputs and outputs are dual-rail encoded. The current control switches and the reference voltages are the structural characteristics that differentiate TSEL from other adiabatic logic families.

The operation of a TSEL PMOS gate has two phases: *discharge* (D_P) and *evaluate* (E_P). Figure 7 shows these phases with respect to the power-clock V_{PC} . During D_P , the energy stored in the capacitance of nodes $\overline{\text{out}}$ or out is recovered. In the beginning of this phase, V_{PC} is high. As V_{PC} starts ramping down toward low, it pulls both V_{out} and $V_{\overline{\text{out}}}$ down toward the PMOS threshold voltage $|V_{tp}|$. This event is adiabatic until V_{PC} drops below $V_{RP} - |V_{tp}|$.

The output of the gate is evaluated during E_P . Let us assume that V_{in} is high and $V_{\overline{in}}$ is low. Initially, V_{PC} is low. As V_{PC} starts rising, MP1 and MP2 turn on. While $V_{PC} < V_{RP} - |V_{tp}|$, MP3 and MP4 are conducting. Since V_{RP} exceeds V_{PC} , a pull-

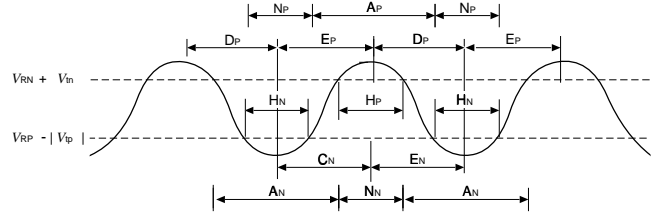


Fig. 7. TSEL timing. D_P : PMOS discharge phase; E_P : PMOS evaluate phase; C_N : NMOS charge phase; E_N : NMOS evaluate phase; H_P, H_N : PMOS and NMOS output held stable; A_P, A_N : adiabatic switching for PMOS and NMOS; N_P, N_N : non-adiabatic switching for PMOS and NMOS.

up path is created from RP to $\overline{\text{out}}$, and the voltage at $\overline{\text{out}}$ starts rising toward V_{RP} . The pair of cross-coupled transistors MP1 and MP2 functions as a sense-amplifier and boosts the voltage difference of the two output nodes. As soon as this difference exceeds $|V_{tp}|$, MP1 turns off and $\overline{\text{out}}$ is charged adiabatically from that point on. When $V_{PC} \geq V_{RP} - |V_{tp}|$, MP3 and MP4 turn off and disconnect the function blocks from the outputs out and $\overline{\text{out}}$. Hence, any further changes in the inputs do not propagate to the outputs. out stays at $|V_{tp}|$ throughout E_P , and $\overline{\text{out}}$ is charged up to the peak of V_{PC} at the end of E_P . The output values are ready to be sampled near the peak of V_{PC} .

The TSEL inverter in Figure 6(b) shows the basic structure of an NMOS gate in TSEL. This gate includes only NMOS devices that are interconnected in a manner identical to its corresponding PMOS gate. The reference voltage level V_{RN} can be selected to maximize the gate's energy efficiency. The gate will still function correctly, however, even if V_{RN} is set equal to V_{RP} .

The operation of an NMOS gate is complementary to PMOS. During each clock cycle, each NMOS gate goes through a *charge* (C_N) phase and an *evaluate* (E_N) phase. During E_N , a pull-down path is formed from an output to RN as long as $V_{PC} > V_{RN} + V_{tn}$, where V_{RN} and V_{tn} are the reference voltage and the threshold voltage for NMOS gates, respectively. When $V_{PC} \leq V_{RN} + V_{tn}$, the current control switches disconnect the function blocks from the outputs, and the recovery of the energy stored in one of the output nodes is initiated. Any further changes to the inputs do not affect the final output values which are sampled near the nadir of V_{PC} .

B. TSEL Energetics

The reference voltage levels V_{RP} and V_{RN} enable the cascading of TSEL gates without any intermediate inverters. These voltages affect the energy dissipation of the TSEL structures, and their optimal values depend primarily on the operating frequency and the output loads of the gates. As V_{RP} decreases, the duration of the non-adiabatic event N_P in the PMOS gates is becoming shorter and the voltage difference between the discharged output nodes and RP decreases. Symmetrically, as V_{RN} increases, the duration of the non-adiabatic event N_N and the voltage difference between the charged output nodes and RN decreases. Consequently, the voltage levels V_{RP} and V_{RN} control both the duration of the evaluation phase and the value of the charging or discharging current, thus affecting the energy dissipation associated with the non-adiabatic intervals during evaluation.

Increasing V_{RP} or decreasing V_{RN} speeds up operation with-

out incurring the area overhead associated with sizing. On the other hand, the closer V_{RP} and V_{RN} are to 0V and V_{dd} , respectively, the lower the energy dissipation of the TSEL cascade is. If V_{RP} drops below a certain value, however, or if V_{RN} exceeds a certain value, the hold stages become too short, and the cascade fails. The theoretical minimum value for V_{RP} is $2 \cdot |V_{tp}|$, whereas the theoretical maximum for V_{RN} is $V_{dd} - 2 \cdot V_{tn}$. Due to this restriction on the scaling of V_{RP} and V_{RN} , the energy efficiency of TSEL at low frequencies degrades. This limitation, which we discuss in more detail with the help of simulation results in Section VI, is remedied in SCAL by the introduction of a tunable current source.

C. TSEL Cascades

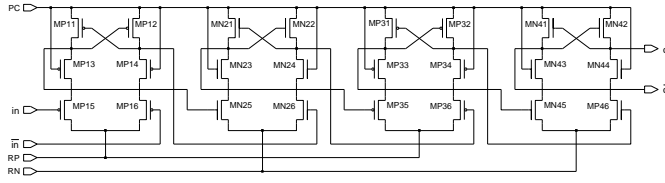


Fig. 8. A 4-stage pipeline of TSEL inverters with two DC reference voltages.

TSEL cascades are built by stringing together alternating PMOS and NMOS gates, as shown in Figure 8. The only signal required to control a TSEL cascade is a single phase of a sinusoidal power-clock. Even though a single reference voltage suffices to ensure correct operation, speed and energy-efficiency can improve by using separate PMOS and NMOS reference voltages.

The relative timing of the gates in a TSEL cascade is shown in Figure 7. At any time during the circuit's operation, either all PMOS gates evaluate and all NMOS gates charge or all PMOS gates discharge and all NMOS gates evaluate. The brief time interval between evaluate/discharge or evaluate/charge during which the outputs of a gate are stable is called the *hold* (H_P or H_N) phase in that gate's operation. While the outputs of the odd stages are stable, their current switches are off. At the same time, the function blocks of the even stages are connected to their reference voltage and can safely evaluate their outputs. After half a cycle, while the current switches of the even stages are off, the function blocks of the odd stages are connected to their reference voltage. Thus, the outputs of the even stages are stable, and the outputs of the odd stages can be evaluated.

IV. SOURCE-COUPLED ADIABATIC LOGIC

This section describes SCAL, a partially adiabatic, dynamic logic family. SCAL retains all of TSEL's positive features, including single-phase power-clock operation. Moreover, it achieves energy efficient operation across a broad range of operating frequencies by using an individually tunable current source at each gate.

A. SCAL Gates

Figure 9 shows the structure of a PMOS and an NMOS inverter in SCAL. The PMOS inverter in Figure 9(a) comprises a pair of cross-coupled transistors (MP1 and MP2), a pair of current control switches (MP3 and MP4), two function blocks

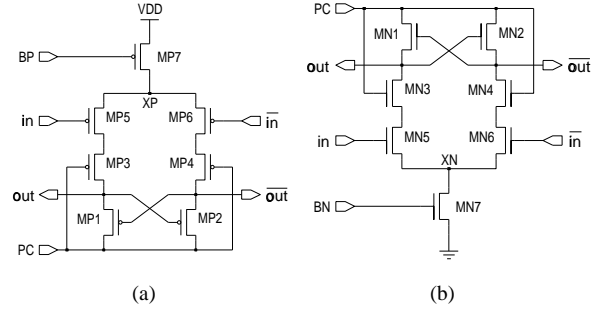


Fig. 9. (a) A PMOS and (b) an NMOS inverter in SCAL.

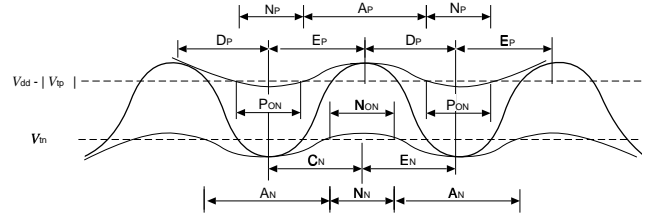


Fig. 10. SCAL timing. D_P : PMOS discharge phase; E_P : PMOS evaluate phase; C_N : NMOS charge phase; E_N : NMOS evaluate phase; P_{ON}, N_{ON} : PMOS and NMOS current source conducting; A_P, A_N : adiabatic switching for PMOS and NMOS; N_P, N_N : non-adiabatic switching for PMOS and NMOS.

(MP5 and MP6), and a current source (MP7) that is biased by a voltage V_{BP} . A sinusoidal power-clock V_{PC} is applied through the port PC. A constant supply voltage V_{dd} is required for activating the pair of cross-coupled transistors. The rate of the charge flow through the current source is controlled by the W/L ratio of MP7.

A PMOS SCAL gate operates in two phases: *discharge* (D_P) and *evaluate* (E_P). Figure 10 shows these phases with respect to the waveform V_{PC} , which is denoted by the bold waveform. The thin waveforms above and below V_{PC} indicate two possible choices for the biasing voltages V_{BP} and V_{BN} , respectively. These waveforms are obtained by level shifting the power-clock V_{PC} and result in increased energy efficiency. SCAL gates will still work with a constant biasing voltage, although at a reduced efficiency level.

The energy stored in the node $\overline{\text{out}}$ or $\overline{\text{out}}$ is recovered during D_P . In this phase, V_{PC} starts from high and ramps down toward low, pulling both $\overline{\text{out}}$ and $\overline{\text{out}}$ down toward the PMOS threshold voltage $|V_{tp}|$. This state change occurs adiabatically until V_{PC} drops below $|V_{tp}|$.

Each PMOS gate computes a new output during the E_P phase. In the beginning of this phase, V_{PC} is low. As V_{PC} starts rising, V_{BP} follows. As long as the gate-to-source voltage $V_{dd} - |V_{BP}|$ of the PMOS current source MP7 exceeds $|V_{tp}|$, MP7 is turned on and the current through MP7 starts raising the voltage V_{XP} of the internal node XP. While $V_{PC} < V_{XP} - |V_{tp}|$, MP3 and MP4 are conducting. Therefore, assuming that V_{in} is high and V_{in} is low, a pull-up path is created from VDD to $\overline{\text{out}}$ via XP, and V_{out} starts rising toward V_{XP} as V_{PC} rises. The cross-coupled transistors MP1 and MP2 turn on and boost the voltage difference between the two output nodes. As soon as this difference exceeds $|V_{tp}|$, MP1 turns off and $\overline{\text{out}}$ is charged adiabatically through MP2.

When $V_{PC} > V_{XP} - |V_{tp}|$, MP3 and MP4 turn off and disconnect the function blocks from the output nodes $\overline{\text{out}}$ and $\overline{\text{out}}$. Hence, any further changes in the inputs do not propagate to the outputs. At the end of the evaluation, $\overline{\text{out}}$ has been charged up to the peak of V_{PC} . The voltage swing of the output is from V_{dd} to $|V_{tp}|$. The output logic values can be sampled near the peak of V_{PC} .

The inverter in Figure 9(b) shows the basic structure of a SCAL NMOS gate. The operation of the NMOS gate is similar to PMOS. The two phases in its operation are *charge* (C_N) and *evaluate* (E_N).

B. SCAL Energetics

The impact of the various circuit parameters on the operation of SCAL can be best understood by examining the behavior of an simplest MOS model in the linear, saturation, and cutoff region. The following equations describe the I-V characteristics in these regions, respectively.

$$I_{ds} = \begin{cases} \frac{k}{2} [2(V_{gs} - V_t)V_{ds} - V_{ds}^2] & V_{gs} \geq V_t, V_{ds} \leq V_{gs} - V_t \\ \frac{k}{2} (V_{gs} - V_t)^2 & V_{gs} \geq V_t, V_{ds} > V_{gs} - V_t \\ 0 & V_{gs} < V_t, \end{cases}$$

where I_{ds} is the drain-to-source current, V_{gs} is the gate-to-source voltage or biasing voltage, V_{ds} is the drain-to-source voltage, V_t is the threshold voltage of device, k (the so-called device transconductance parameter) is defined as $k = \mu C_{ox} (W/L)$, μ is the effective surface mobility of the carrier in the channel, and C_{ox} is the gate-oxide capacitance per unit area. From this equation it follows that the turning of a current source on or off is controlled by the biasing voltage. Moreover, the amount of current through a current source is proportional to the biasing voltage and the W/L ratio of the current source.

In SCAL, the dissipative current through the current source of each gate is used to activate the cross-couple transistors. Even though all the gates of the same type have the same biasing voltage, the amount of current through each gate's current source is individually controlled by the W/L ratio of the current source. Thus, minimum dissipation can be achieved under any given operating conditions, such as output load or operating frequency, by adjusting the individual W/L ratios of the SCAL gates.

The main difference in the operation of SCAL and TSEL is in the method that controls the current activation of the cross-coupled transistors during the evaluation phase. The energy efficiency of TSEL gates at low frequencies is limited by the limit to the scaling of the DC reference voltages. SCAL has no such limitation, however, because the magnitude of the current flow at the beginning of the E_P (or E_N) phase can be controlled by adjusting the W/L ratio of MP7 (or MN7) in each gate. At the same time, the duration of the E_P (or E_N) phase is determined independently of the current flow by selecting a biasing voltage that is shared by all PMOS (or NMOS) gates. Thus, for any operating frequency, each SCAL gate can be individually tuned to achieve minimum dissipation under its output load.

C. SCAL Cascades

To build SCAL cascades, PMOS and NMOS gates are chained alternatively. The only signal required to control a

SCAL cascade is a power-clock V_{PC} . To improve the energy efficiency of the cascade, two biasing voltages V_{BP} and V_{BN} can be used that are obtained by shifting the level of V_{PC} . The speed and energy efficiency of a SCAL cascade can be tuned by optimally sizing the current source in each gate. Since individual gates can be tuned independently, efficient operation can be achieved for a broad range of operating frequencies. Energy consumption is minimized by setting the W/L ratio of each current source equal to the minimum possible value and by bringing the biasing voltage of PMOS and NMOS current source close to the PMOS and NMOS threshold voltage, respectively. This section describes the operation of SCAL cascades and explains the dependence of their efficiency on the size of the current source through HSPICE simulation results.

Figure 10 shows the timing of the signals in a SCAL cascade. At any time during the circuit's operation, either all PMOS gates evaluate and all NMOS gates charge or all PMOS gates discharge and all NMOS gates evaluate. The brief time interval between evaluate/discharge or evaluate/charge during which the outputs of a gate are stable is called the *hold* (H_P or H_N) phase in that gate's operation. While the current switches of the odd stages are off, their outputs are stable. At the same time, the function blocks of the even stages are connected to VDD (or VSS) through the current sources and can safely evaluate their outputs. After half a cycle, while the current switches of the even stages are off, the inputs of the odd stages are stable, and their function blocks are connected to VSS (or VDD) through their current sources.

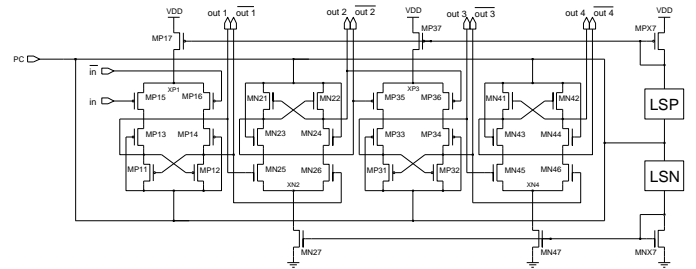


Fig. 11. A 4-stage pipeline of SCAL inverters and associated biasing circuitry.

A PNP cascade of SCAL inverters and its biasing circuitry for the current sources are shown in Figure 11. The blocks denoted by LSP and LSN are voltage level shifters that generate the biasing voltage for the PMOS and NMOS gates, respectively.

Figure 12 shows the input and output waveforms obtained from HSPICE simulations of the 4-stage pipeline from Figure 11. These simulation results were obtained when a periodic sequence "...0111..." was propagated through the inverter chain at 100MHz. The W/L ratio for the pair of cross-coupled transistors was 5/2. For the function blocks, we used minimum-size transistors from a $0.5\mu\text{m}$ standard CMOS technology with a W/L ratio equal to 3/2. For the current sources MP17, MN27, MP37 and MN47, the W/L ratios were 1/2, 1/4, 2/1 and 1/1, respectively.

Figure 13 shows the internal voltages and source currents for each stage in the 4-stage pipeline of SCAL inverters from Figure 11. The internal voltages V_{XP1} , V_{XN2} , V_{XP3} , and V_{XN4} and

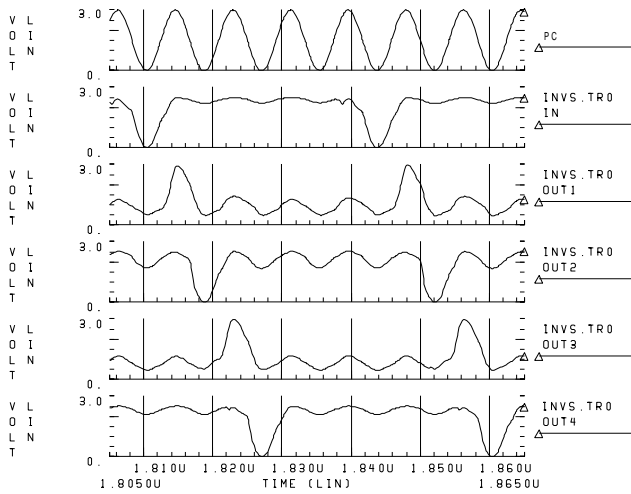


Fig. 12. Waveforms obtained from HSPICE simulations of the 4-stage SCAL pipeline from Figure 11. From top to bottom: (1) power-clock V_{PC} , (2) input of 1st stage, (3) output of 1st stage, (4) output of 2nd stage, (5) output of 3rd stage, and (6) output of 4th stage.

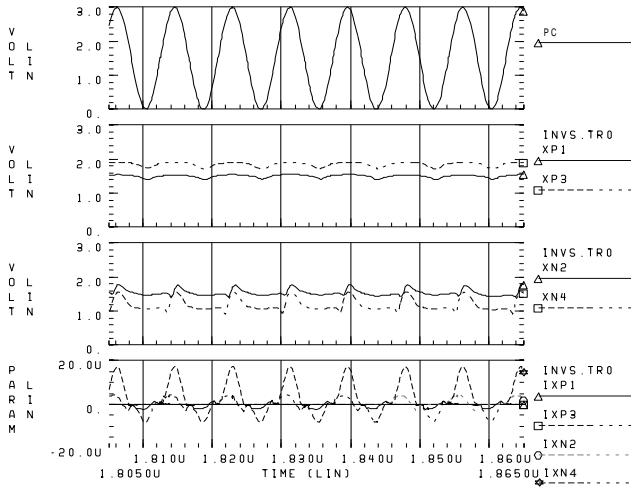


Fig. 13. Waveforms obtained from HSPICE simulations of the 4-stage SCAL pipeline from Figure 11. From top to bottom: (1) power-clock V_{PC} , (2) internal voltages V_{XP1} and V_{XP3} , (3) internal voltages V_{XN2} and V_{XN4} , (4) currents through the current sources MP17, MN27, MP37, and MN47.

the internal source currents I_{XP1} , I_{XN2} , I_{XP3} , and I_{XN4} are proportional to the transistor ratios in the corresponding current sources. These voltages and currents affect the speed and energy dissipation of the SCAL structures. As the W/L ratio of a current source transistor in a gate decreases, the current that activates its cross-coupled transistors also decreases. Conversely, as the W/L ratio increases, current flow during the non-adiabatic event of the gate increases. Individual tuning of the current source sizes at each gate can thus decrease the energy dissipation of the cascade.

V. ADDER DESIGNS

In order to evaluate the energy efficiency of TSEL and SCAL, we designed a collection of CLAs using static CMOS, TSEL, SCAL, PAL, and 2N2P. All CLAs had the same gate-level structure but differed in aspects that were specific to the logic styles used in their design. This section describes our various adder

designs that were all developed in $0.5\mu\text{m}$ standard CMOS technology.

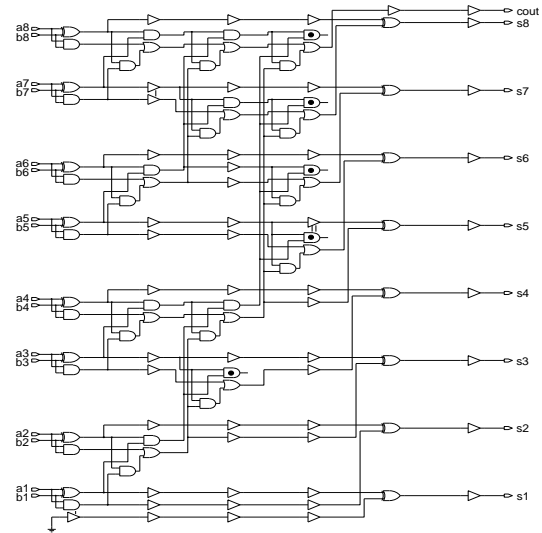


Fig. 14. Schematic diagram of 8-bit CLA.

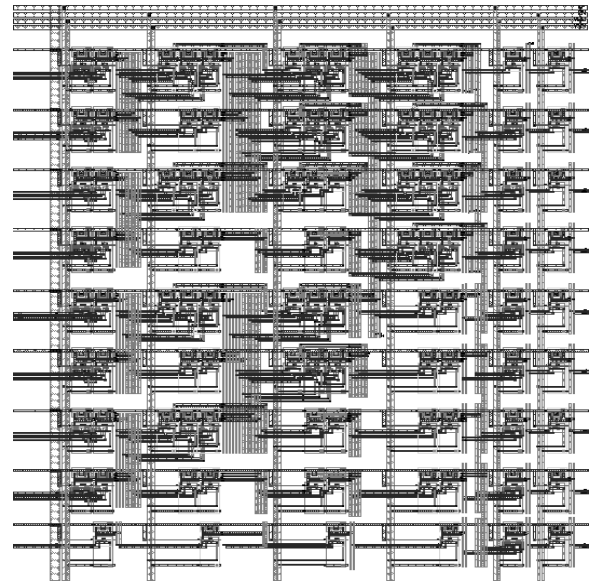


Fig. 15. Full-custom layout of 8-bit CLA in TSEL.

The gate-level schematic diagram used to develop the 8-bit CLA in static CMOS, PAL, 2N2P, TSEL and SCAL is shown in Figure 14. The buffers shown are used to propagate the correct logic values in PAL, 2N2P, TSEL, and SCAL and are not included in static CMOS. Dummy cells, indicated by dots in the schematic diagram, are included to regularize the full-custom layouts of the adiabatic logic families.

The full-custom layouts of the 8-bit CLAs we designed in TSEL and SCAL are shown in Figure 15 and Figure 16. Both designs have almost the same number of devices: 778 transistors for TSEL and 877 transistors for SCAL. The slight difference in the transistor counts of the two designs stems from the inclusion of a current source at each SCAL gate. The area of each of these CLAs is approximately 0.33 mm^2 .

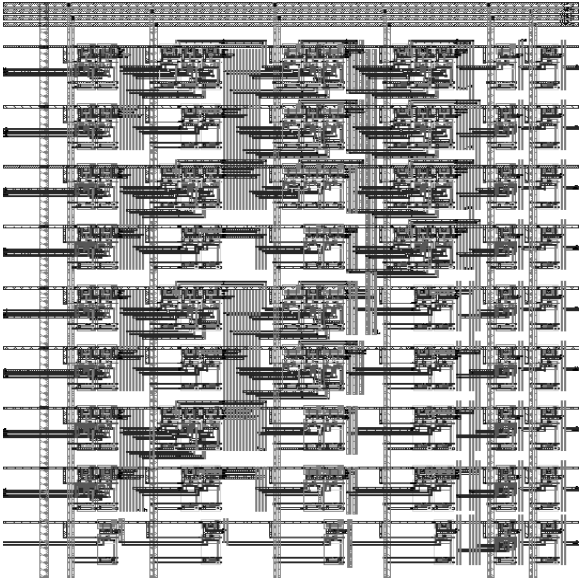


Fig. 16. Full-custom layout of 8-bit CLA in SCAL.

Both the TSEL and the SCAL CLA generate a new output on each clock cycle. Each adder has a latency of 3.0 cycles, since data propagation through each gate takes half a cycle. In the SCAL adder, the W/L ratio of each current source was selected individually among the values $1/8$, $1/4$, $1/2$, $1/1$, $2/1$, $4/1$, and $8/1$, according to the operating frequency, the number of inputs to the gate, and the capacitive load at the output of the gate. For the function blocks of each gate, minimum-size transistors were used with W/L ratio equal to $3/2$. The W/L ratios of the cross-coupled transistors was set to $10/2$ in every gate.

The 2N2P and PAL CLAs were obtained directly from the TSEL/SCAL designs by introducing additional clock lines and replacing the TSEL/SCAL gates by their corresponding gates in the other adiabatic styles. The area taken by their full-custom layouts was comparable with that of the TSEL/SCAL designs. The W/L ratios of the function blocks and the cross-coupled transistors were the same as in the TSEL/SCAL CLAs. All primary outputs were connected to a 60fF load.

Both the 2N2P and the PAL adders have the same throughput as the TSEL/SCAL design, generating a new output on each clock cycle. The latency of the PAL adder is 3.0 cycles. The latency of the 2N2P CLA is 1.5 cycles, however, since data propagation through each 2N2P gate takes 0.25 cycle.

In addition to the adiabatic CLAs, we developed two CLAs in static CMOS based on the gate-level schematic diagram shown in Figure 14. The first CMOS design was a purely combinational CLA. The second CMOS adder was a pipelined version of the fully combinational one with 3 pipeline stages. The standard-cell layouts of these two designs were generated using EPOCH in a $0.5\mu\text{m}$ standard CMOS technology. All transistors in the evaluation trees of both CMOS adders were minimum size. To meet the timing constraints, a buffer was introduced at the output of each gate in the fully combinational CLA. Similarly, a buffer was introduced after each register in the pipelined CLA. In both cases, the W/L ratio of each buffer was $10/2$.

VI. SIMULATION RESULTS

In this section, we present HSPICE simulation results for the 8-bit CLAs we developed in static CMOS, PAL, 2N2P, TSEL, and SCAL. Our circuits were designed in a $0.5\mu\text{m}$ standard CMOS technology and were simulated with distributed-RC parameters extracted from layout. The simulations accounted for the dissipation of the gates and internal clock lines, assuming a 100% energy-efficient clock generator.

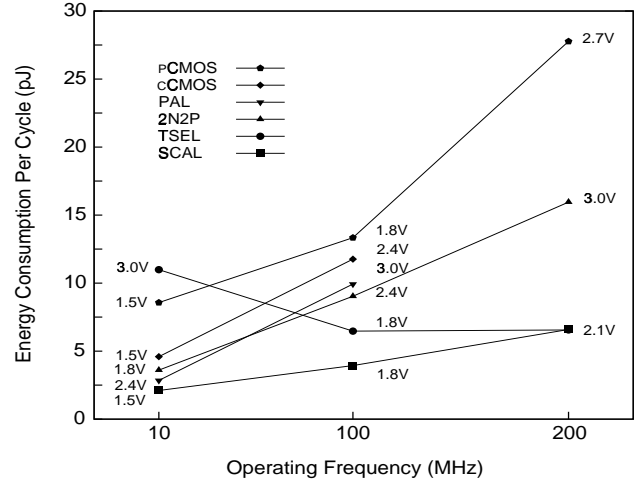


Fig. 17. Energy consumption per cycle vs. operating frequency for 8-bit CLAs.

Figure 17 gives the per-cycle energy consumption of our adders operating at 10MHz, 100MHz, and 200MHz. For each operating frequency, the minimum energy dissipation of each adder was obtained using the smallest supply voltage that ensured its correct function at that frequency. Reference and biasing voltages were determined by trial and error. The supply voltages used are shown next to their corresponding data points. The minimum possible supply voltage dictated by the process parameters was 1.5V. In general, SCAL possesses excellent voltage scaling properties. For every operating point, it can operate with the lowest supply voltage among all the adders we have designed.

Our results show that SCAL is more energy efficient than the other adiabatic logic families and both static CMOS designs across the entire frequency range of our simulations. At 10MHz, SCAL is 1.5 to 2 times more energy efficient than the other adiabatic designs. Moreover, it is 2 times more energy efficient than the purely combinational CMOS CLA (denoted by cCMOS) and 3 times more energy efficient than the 3-stage pipelined CMOS CLA (denoted by pCMOS). At 100 MHz, the SCAL CLA is at least 2 times more energy efficient than the other adiabatic designs and 2 to 3 times more energy efficient than the two CMOS designs. At 200MHz, the SCAL CLA is about 2.5 times more energy efficient than 2N2P and almost 5 times more energy efficient than pCMOS. The PAL and cCMOS CLAs do not function correctly at that frequency.

The TSEL adder is less dissipative than the PAL, 2N2P, and both CMOS designs for operating frequencies above 100MHz. Its dissipation increases sharply at 10MHz, however, because at such a low operating frequency the two DC reference voltages used in the adder reach their limits, as discussed in Subsection

III-B. Consequently, the duration of the evaluation phase increases, resulting in higher overall energy consumption.

Neither the fully adiabatic PAL adder nor the pipelined static CMOS adder perform better than SCAL. The PAL adder, which is geared for very energy efficient operation at low frequencies, is more dissipative than SCAL even at 10MHz and stops functioning above 100MHz. The pipelined CMOS adder is more dissipative than every other design, except for TSEL at 10MHz. The flip-flops used to reduce path delays and decrease the required supply voltage in pCMOS end up increasing the circuit's effective capacitance and thus limit energy savings. Thus, SCAL presents a promising approach to further reducing the dissipation of CMOS designs that have reached their voltage scaling limits.

The internal node capacitances of the adiabatic designs we used in our experiments were roughly equal. Thus, a clock generator with efficiency less than 100% would merely shift the dissipation values of the adiabatic designs without changing their relative order or ratio. The relative energy savings with respect to CMOS would be lower, however, for all adiabatic families.

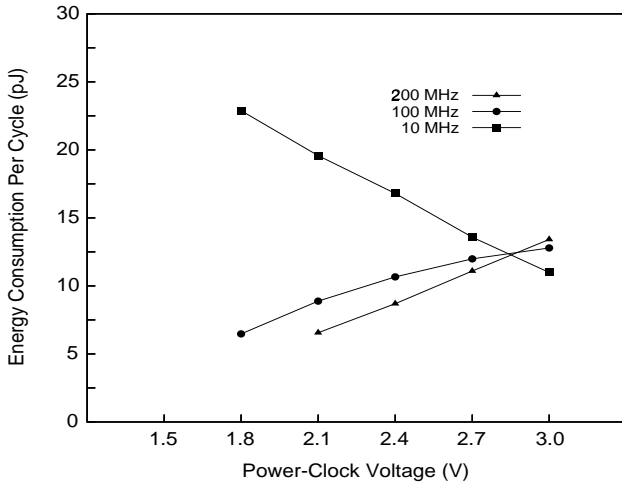


Fig. 18. Energy consumption vs. peak power-clock voltage for 8-bit TSEL CLA.

Figure 18 reveals a paradox in the operation of TSEL: Energy consumption decreases with increasing voltage swing! The graphs in this figure show the energy consumption of the TSEL adders for 10MHz, 100MHz, and 200MHz as a function of the peak power-clock voltage. Each point was obtained with optimal reference voltages V_{PR} and V_{NR} that were computed by trial and error. At 200MHz and 100MHz, as the peak power-clock voltage decreases, the energy dissipation also decreases. At 10MHz, however, energy consumption decreases by increasing the peak power-clock voltage.

This seemingly counterintuitive behavior can be explained with the help of the waveforms in Figure 19. Both power-clock waveforms in this figure have a 10MHz frequency. At such a low operating frequency, the DC reference voltages have already reached the minimum values that allow correct circuit function. Therefore, the duration of the evaluation phases cannot be controlled by adjusting the reference voltage values and can thus be excessively long, resulting in higher overall energy consumption. By increasing the peak power-clock voltage, the evaluation

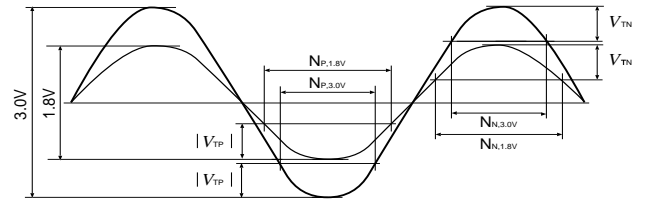


Fig. 19. Adjustment of non-adiabatic switching interval in TSEL by voltage scaling.

phases become shorter. This fact is straightforward to verify by comparing the lengths of the intervals $N_{P,3.0V}$ and $N_{P,1.8V}$ that correspond to the non-adiabatic switching stages for PMOS at 3.0V and 1.8V, respectively. The reduction in the length of the non-adiabatic stage offsets any increased energy losses due to the higher voltage swing. Thus, the overall energy efficiency of the TSEL gates increases.

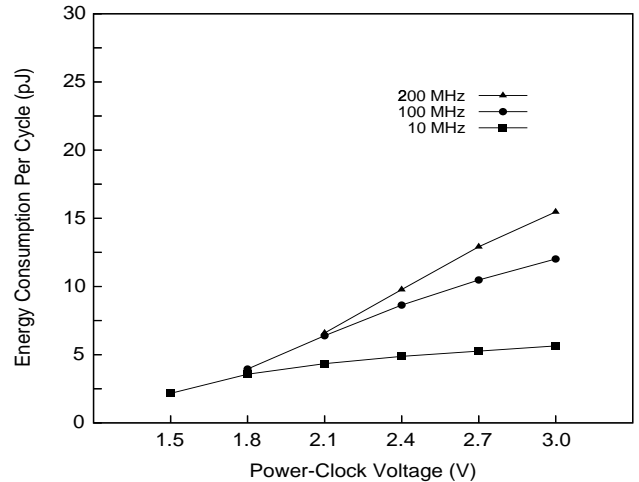


Fig. 20. Energy consumption vs. peak power-clock voltage for 8-bit SCAL CLA.

Contrary to TSEL, the operation of the SCAL adder under voltage scaling follows common wisdom. Figure 20 shows the energy dissipation of three SCAL adders as a function of the power-clock voltage. Each of the three adders was derived by tuning the current sources of the original adder design for minimum energy dissipation at 10MHz, 100MHz, and 200MHz. For example, the SCAL adder at 10MHz was optimized for a 1.5V power-clock voltage. Similarly, the adders simulated at 100MHz and 200MHz were optimized for supply voltages of 1.8V and 2.1V, respectively. As expected, the energy consumption of the adders increases monotonically as their peak power-clock voltage increases. Moreover, as their operating frequencies increase, their dissipation becomes more sensitive to changes in the power-clock voltage.

VII. CONCLUSION

We presented the first-ever true single-phase adiabatic logic family with a broad operating range. The simplest member of our family is TSEL. The other member of our family is SCAL, a source-coupled variant of TSEL that achieves increased energy efficiency by using a tunable current source to control the

rate of charge flow into or out of each gate. Our adiabatic circuitry avoids a number of problems associated with multiple power-clock schemes, including increased energy dissipation, layout complexity in clock distribution, clock skew, and multiple power-clock generators.

In HSPICE simulations of layouts in a standard $0.5\mu\text{m}$ CMOS technology, TSEL and SCAL adders outperformed corresponding designs in static CMOS, PAL and 2N2P that were operating with power-clock voltages scaled for minimum energy dissipation. In comparison with static CMOS, PAL, and 2N2P, SCAL was 1.5 times more energy efficient at 10MHz and at least 2 times more energy efficient at higher operating frequencies. Moreover, our SCAL adders were 2 to 5 times more energy-efficient than corresponding combinational and pipelined CMOS designs in the 10–200MHz range. TSEL was less dissipative than PAL, 2N2P, and both CMOS designs for operating frequencies above 100MHz. Although our single-phase designs were tuned manually by trial and error, the results of our investigation suggest that TSEL and SCAL are excellent candidates for high-speed and low energy VLSI design.

We have recently designed an 8×8 SCAL multiplier with built-in self-test (BIST) and a single-phase sinusoidal power-clock generator with a surface mount inductor. Although the resonant clock drivers proposed by most previous papers can be used to generate a single-phase power-clock, we designed our own single-phase generator that resembles a zero-voltage switched resonant power converter. A key feature of our generator is that it only conducts a small fraction of the entire inductor current. We have also developed a set of CAD tools for automating the verification and optimization of large adiabatic designs. Our chip has been fabricated in a standard $0.5\mu\text{m}$ CMOS process and is currently being tested.

ACKNOWLEDGMENTS

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