EECS 211
CAD Assignment 4: CMOS Inverter

Goal: To simulate a CMOS inverter using Accusim and to compare the simulated characteristics with the hand calculations. To see that different levels of SPICE models have different levels of accuracy, and that level 1 models in general match the hand calculations. Level 3 models take into consideration second order effects not taken into account by the hand calculations, and therefore are much more accurate.

Refer to the previous section on modeling a CMOS inverter in Accusim and model a CMOS inverter in a 1.2 um technology with $k_n^* = 81 \text{ uA/V}^2$ and $k_p^* = 27 \text{ uA/V}^2$, $V_{dd} = 5\text{V}$, $V_t = 0.75$, with $(W/L)_n = 1.5$ and $(W/L)_p = 4.5$.

1. For the NMOS transistor calculate $C_{GS}$, $C_{GD}$, $C_{DB}$ for $V_{DS} = 4.8\text{V}$ (saturation) and $V_{DS} = 0.2\text{V}$ (triode). In both cases, $V_{GS} = 5\text{V}$. Do not forget the overlap capacitance knowing that $L_{OV} = 0.2\text{um}$. Take $C_{DB}(0) = 40\text{fF}$ and $t_{ox} = 25\text{nm}$. Put all your calculated values in a table.

2. Using Accusim, determine the $V_o$ versus $V_i$ transfer function. Make a table comparing the $V_{OH}$, $V_{OL}$, $V_{IH}$, $V_{IL}$ of the level 1 model, level 3 model and your calculated values.

   Give one plot (level 3 models) of the transfer characteristic.

3. Using Accusim, determine the transistor switching current ($V_{CC}$ current draw) versus the input voltage. Make a table comparing the peak switching current of the level 1, level 3, and hand calculated values.

   Give one plot (level 3 models) of the current.

4. Put a 500 MHz square wave at the input of the inverter and use the zoom feature to determine the inverter delay ($t_{PLH}$ or $t_{PIL}$). Determine the 10%–90% rise–time and from this value, calculate the 3–dB corner frequency (as in your prelab #1). Knowing that you want to pass the 5th harmonic of a square wave, determine the maximum frequency of operation of the inverter (with no capacitive loads). This frequency is determined by the internal capacitances of the transistors (and their sizes). Make a table comparing the level 1 and the level 3 values.

   Give one plot (level 3 models) of the output voltage versus time.

**Now, put a 100 fF capacitor as your load.**

5. Repeat 4 but with a 100 MHz square–wave at the input. Be careful: $V_i \neq 0.2 \text{V}_{dd}$ and therefore, you need to use the long equation for $t_{PLH}$ found in the textbook.
6. Determine the peak current in the capacitor. Make a table comparing the level 1, level 3, and your hand calculated values.

   Give one plot (level 3 models) of the capacitor current.

Your CAD should be 6 pages and have 5 plots.

**TIP:** You will have to simulate each part with the level 1 and the level 3 models. I recommend you start by simulating with the level 1 models. The values from these simulations will be similar to your hand calculations. Now, recreate your viewpoint with the level 3 models and simulate. Your level 1 and level 3 models will produce different simulation results. The voltage and current values will be similar (part 2 and 3) but the time and frequency values will be very different (part 4 and 5). If your values for the level 1 and level 3 models are the same, you are doing something wrong.

**BIG TIP:** At this point it is assumed that you have learned how to use the Mentor CAD tools. Thus, very little credit will be given for producing plots. Most of the credit will be given for producing and calculating correct values. So, if you don’t know how to calculate a value, ask one of us.