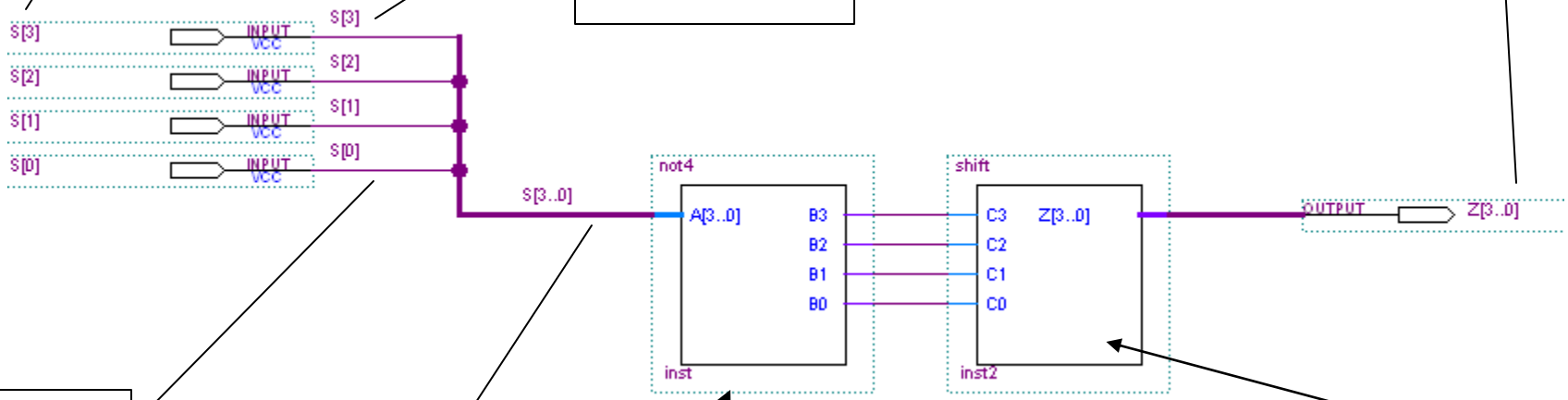
QSF File Assignments

```
set_location_assignment PIN_N25 -to S[0]
set_location_assignment PIN_N26 -to S[1]
set_location_assignment PIN_P25 -to S[2]
set_location_assignment PIN_AE14 -to S[3]
```

QSF File Assignments

```
set_location_assignment PIN_AE23 -to Z[0]
set_location_assignment PIN_AF23 -to Z[1]
set_location_assignment PIN_AB21 -to Z[2]
set_location_assignment PIN_AC22 -to Z[3]
```

Net name is the same name as port (pin) name.



Implement bus taps by naming nets bus member names, i.e. S[1]

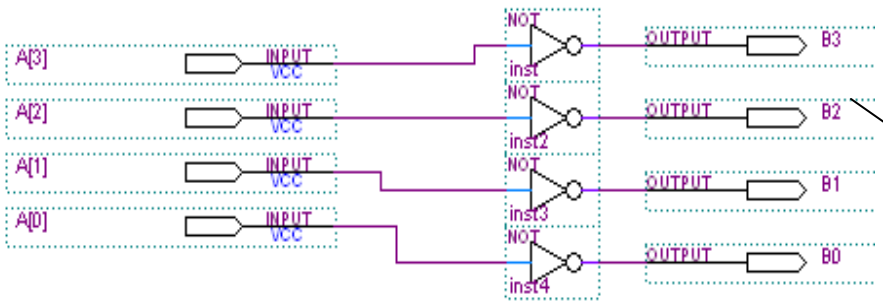
Name schematic buses S[3..0] not, S[3:0]

Verilog Module (bit wise shifter)

```
module shift(C3, C2, C1, C0, Z);
    input C3, C2, C1, C0;
    output [3:0] Z;
    wire [3:0] Z;

    assign Z[1]=C0;
    assign Z[2]=C1;
    assign Z[3]=C2;
    assign Z[0]=C3;
endmodule
```

Schematic Module (bit wise inverter)



Naming as bus members creates bus port on schematic module

Naming as individual members creates individual ports