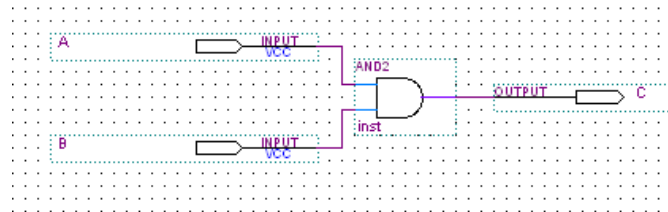


## EECS 270 Quick Reference Simulation Guide



Design File (my\_design.bdf)

```
`timescale 1 ns/1 ns //time scale for the test bench

module my_testbench_module(); // the test bench module

    reg A_s, B_s; //define stimulus input ports
    wire C_s; //define stimulus output port

    //the following connects the test procedure below to my_design
    my_design t1(.A(A_s), .B(B_s), .C(C_s));

    //what follows is the test procedure
    initial begin

        //test all possible input conditions
        //10 means wait 10 time scale units (defined to be ns above)
        A_s <= 0; B_s <= 0; //set 1st test case
        #10; //wait 10ns
        A_s <= 1; B_s <= 0; //set 2nd test case
        #10; //wait 10ns
        A_s <= 0; B_s <= 1; //set 3rd test case
        #10; //wait 10ns
        A_s <= 1; B_s <= 1; //set 4th test case
        #10; //wait 10ns
    end
endmodule
```

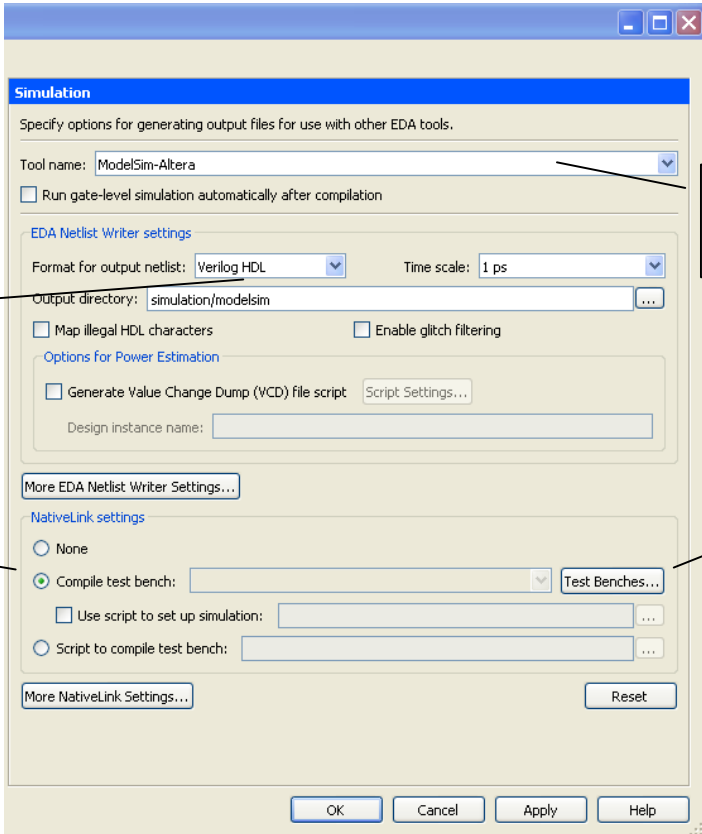
Test Bench File (my\_testbench\_file.v)

### Test Bench Essentials

1. The top level test bench module name "my\_testbench\_module" is arbitrary, but unique.
2. The design file name "my\_design" must be named exactly as the design file name.
3. The instance name "t1" is arbitrary, but unique.
4. The port references (pins) to my\_design must use the same name as the design (A, B and C).
5. The port (variable) references to the simulation must follow the declaration naming and be unique A\_s, etc
6. The output simulation port "C" needs to be declared as a wire.
7. Naming should start with a lower or upper case letter.

## Setting Up the Quartus Project for Simulation

Go To: Assignments→Settings→Simulation and fill the field in accordingly.



The screenshot shows the 'Simulation' dialog box in Quartus. The 'Tool name' is set to 'ModelSim-Altera'. The 'Format for output netlist' is set to 'Verilog HDL'. The 'Time scale' is set to '1 ps'. The 'Output directory' is 'simulation/modelsim'. The 'EDA Netlist Writer settings' section includes checkboxes for 'Map illegal HDL characters' and 'Enable glitch filtering'. The 'Options for Power Estimation' section includes a checkbox for 'Generate Value Change Dump (VCD) file script'. The 'NativeLink settings' section includes radio buttons for 'None', 'Compile test bench', and 'Script to compile test bench'. The 'Compile test bench' option is selected, and the 'Test Benches...' button is highlighted. The 'Design instance name' field is empty. The 'Reset' button is at the bottom right. The 'OK', 'Cancel', 'Apply', and 'Help' buttons are at the bottom.

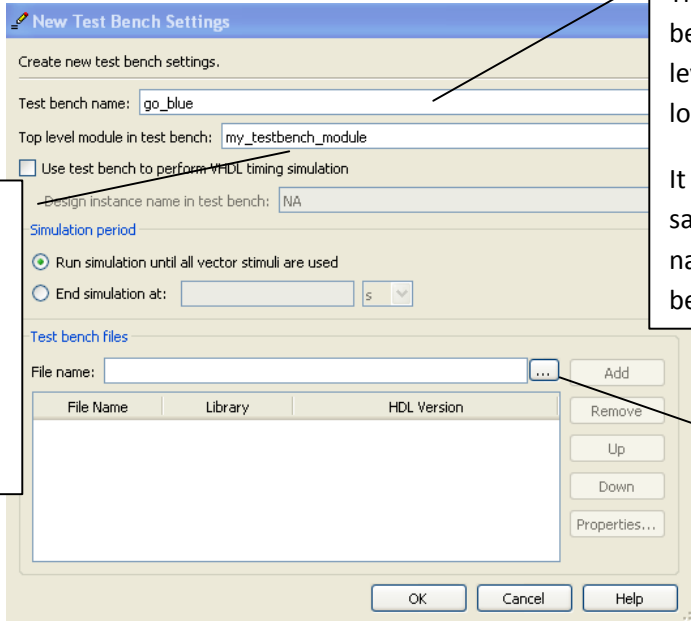
Select the ModelSim-Altera tool

Select Verilog

Select Compile test bench

Select Test Benches to link your test bench module name and file.

Go To: Test Benches and Select New



The screenshot shows the 'New Test Bench Settings' dialog box in Quartus. The 'Test bench name' is 'go\_blue'. The 'Top level module in test bench' is 'my\_testbench\_module'. The 'Design instance name in test bench' is 'NA'. The 'Simulation period' section includes radio buttons for 'Run simulation until all vector stimuli are used' and 'End simulation at:'. The 'Test bench files' section includes a 'File name' field and a table with columns 'File Name', 'Library', and 'HDL Version'. The 'Add' button is highlighted. The 'OK', 'Cancel', and 'Help' buttons are at the bottom.

This field names the test bench and associates the top level module name and file location for the test bench.

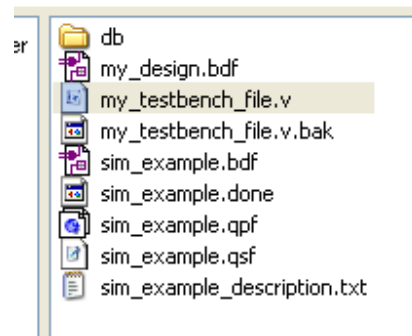
It does NOT have to be the same name as the module name or file name, but can be.

This field **MUST** be named the module name in your test bench file.

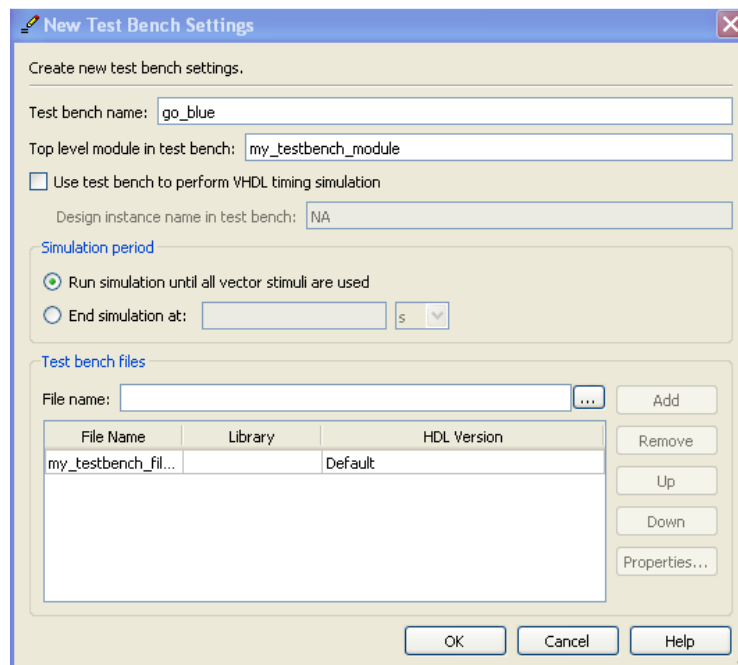
It does NOT have to be the same as the file name or test bench name field, but can be.

Browse to test bench file.

### Browse, Select and Open my\_testbench\_file

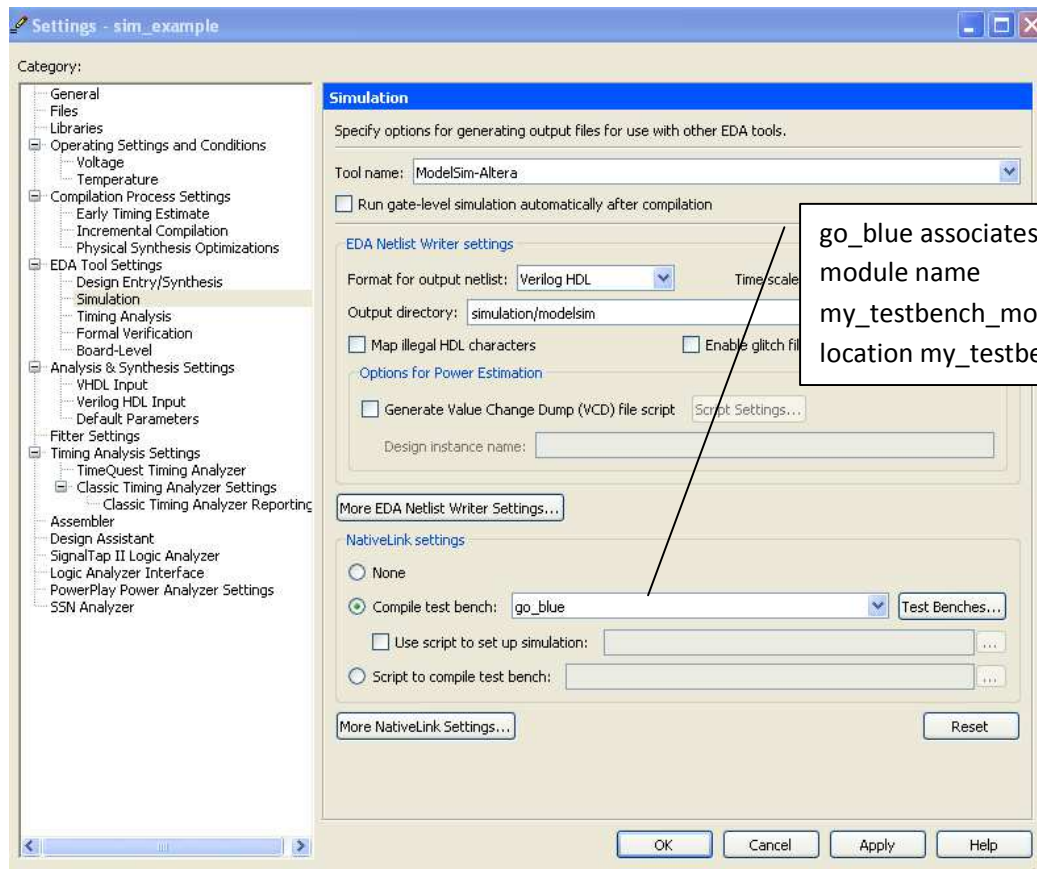


### Add to test bench library



### Acknowledge and return to the Simulation Settings Window

Note you must click APPLY for these setting to be accepted.



### Selecting Timing or Functional Simulation

The default is for Timing Simulation

To Select Functional Simulation, Select “More ED Netlist Writer Settings”

Select On for “Generate netlist for functional simulation only”

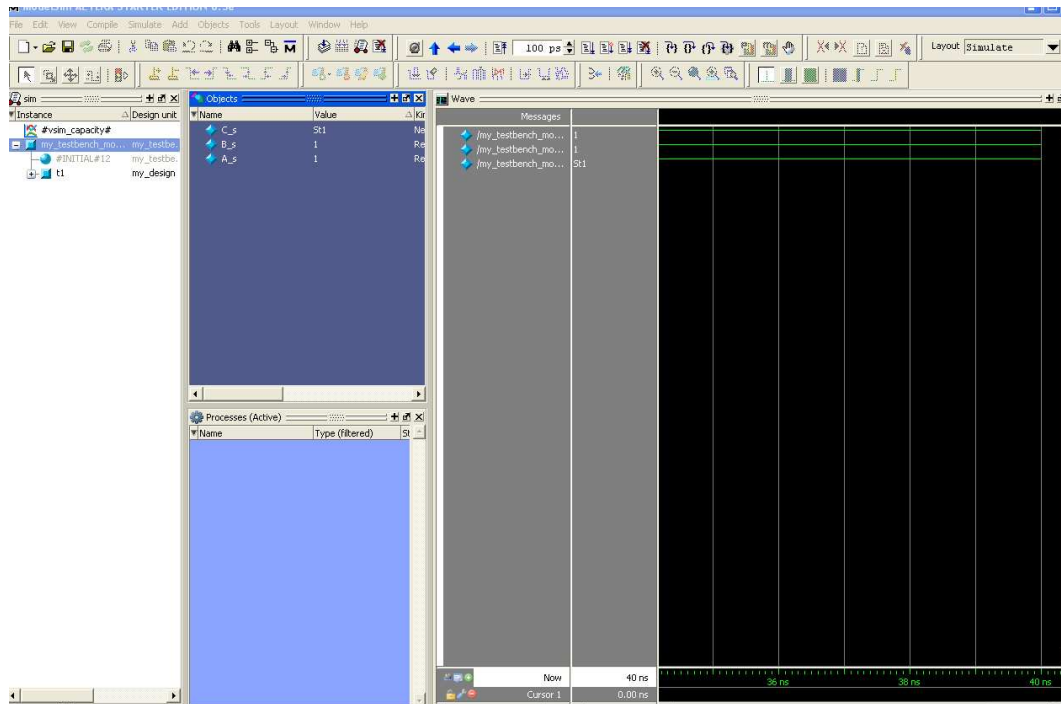
Existing option settings:

Name:	Setting:
Architecture name in VHDL output netlist	structure
Bring out device-wide set/reset signals as ports	Off
Disable detection of setup and hold time violations in the input registers of bi-directional pins	Off
Do not write top level VHDL entity	Off
Flatten buses into individual nodes	Off
Generate netlist for functional simulation only	On
Generate third-party EDA tool command script for RTL functional simulation	Off
Generate third-party EDA tool command script for gate-level simulation	Off
Location of user compiled simulation library	<None>
Maintain hierarchy	Off
Truncate long hierarchy paths	Off

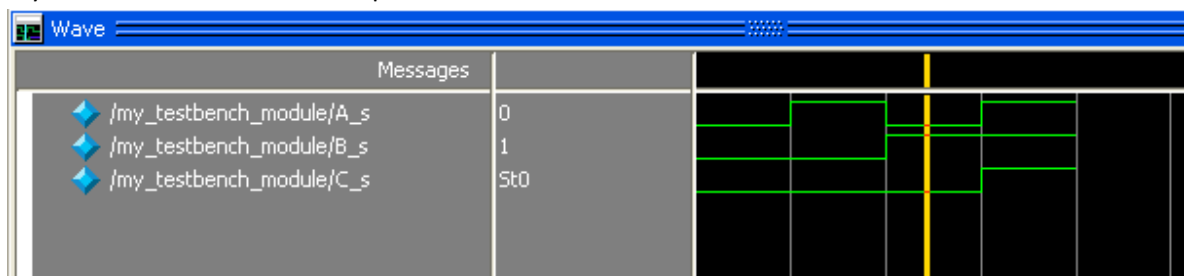
## To Run Simulation

1. Make Sure all Settings Were Saved
2. Processing→Start Compilation
3. Run EDA Simulation Tools→EDA Gate Level Simulation

The following page should open.



Click in the waveform window to activate the cursor, right click and select zoom out or use the minus key. You should be able to manipulate the waveform screen to see the simulation results.



To add a second cursor, click on the plus sign in the lower left waveform window in the signal column. A second cursor will appear. The simulation time point and difference between the 2 cursors is displayed below on the time line.

