

2.80 Design an 8x3 encoder using AND, OR and NOT gates. Assume that only one input will be asserted at any given time.

Inputs								Outputs		
i7	i6	i5	i4	i3	i2	i1	i0	e2	e1	e0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$e2 = I7 + I6 + I5 + I4$$

$$e1 = I7 + I6 + I3 + I2$$

$$e0 = I7 + I5 + I3 + I1$$

