

3.10 Trace the behavior of a level-sensitive SR latch (see Figure 3.14) for the input pattern in Figure 3.73. Complete the timing diagram, assuming logic gates have a tiny but non-zero delay. Assume S1, R1, and Q are initially 0.

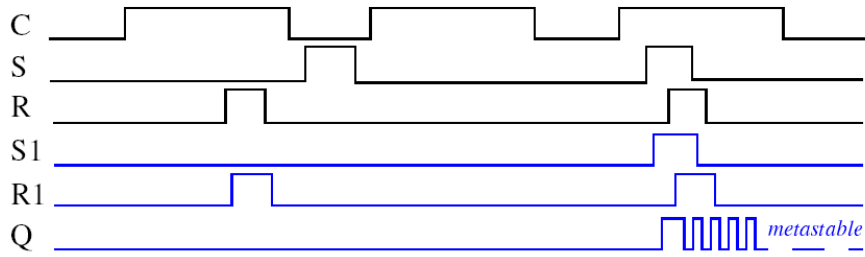


Figure 3.73: SR latch input pattern timing diagram and Solution for Exercise 3.10.