

3.15 Compare the behavior of D latch and D flip-flop devices by completing the timing diagram in Figure 3.78. Provide a brief explanation of the behavior of each device. Assume each device initially stores a 0.

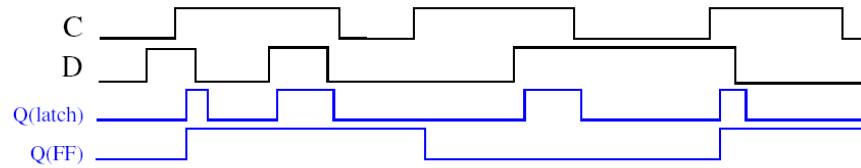


Figure 3.78: D latch and D flip-flop input pattern timing diagram and Solution for Exercise 3.15.

As long as the C (clock) input is 1, the D latch will store the value of D (after a short gate delay). The D flip-flop will only store the value of D on the rising edge of C (after a short gate delay).