

3.30 Trace through the execution of the FSM you created in Exercise 3.29 by completing the timing diagram in Figure 3.84, where C is the clock input and S is the n-bit state register. Assume S is initially 000.

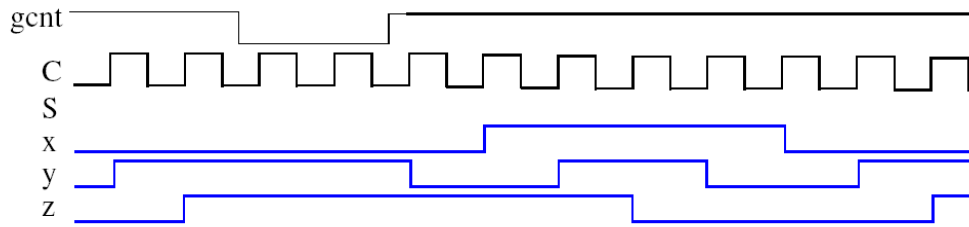


Figure 3.84: FSM input pattern timing diagram and Solution to Exercise 3.30.