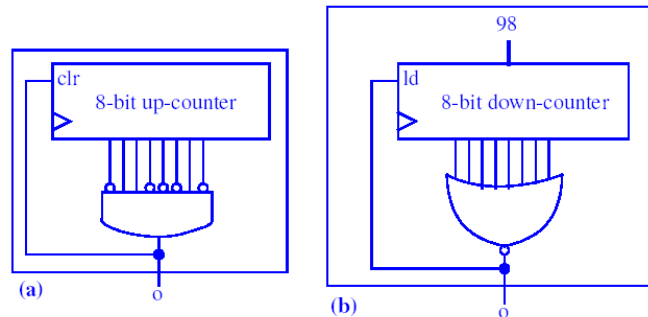


- 4.40 (a) Using an up-counter with a synchronous clear control input, and extra logic, design a circuit that outputs a 1 every 99 clock cycles. (b) Design the counter from part (a), but use a down-counter with parallel load. (c) What are the tradeoffs between the two designs from parts (a) and (b)? (*Component use problem*).



- (c) The circuit we implemented in (a) is a simpler design, while the circuit implemented in (b) is easier to modify to pulse at a different rate.