

- 4.5 Design an 8-bit register with 2 control inputs  $s_1$  and  $s_0$ , 8 data inputs  $I_7..I_0$ , and 8 data outputs  $Q_7..Q_0$ .  $s_1s_0=00$  means maintain the present value,  $s_1s_0=01$  means load, and  $s_1s_0=10$  means clear.  $s_1s_0=11$  means to swap the high nibble with the low nibble (a nibble is 4 bits), so 11110000 would become 00001111, and 11000101 would become 01011100. (*Component design problem*).

