

5.10 (a) Use the RTL design method of Table 5.1 to convert the high-level state machine in Figure 5.94 to a controller and a datapath. Design the datapath to structure, but design the controller to an FSM only. (b) *Design the controller's FSM down to structure.

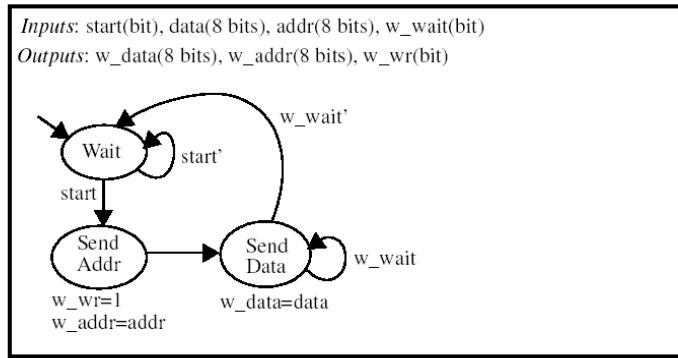


Figure 5.94: High-level state machine of bus interface with bus wait signal.

