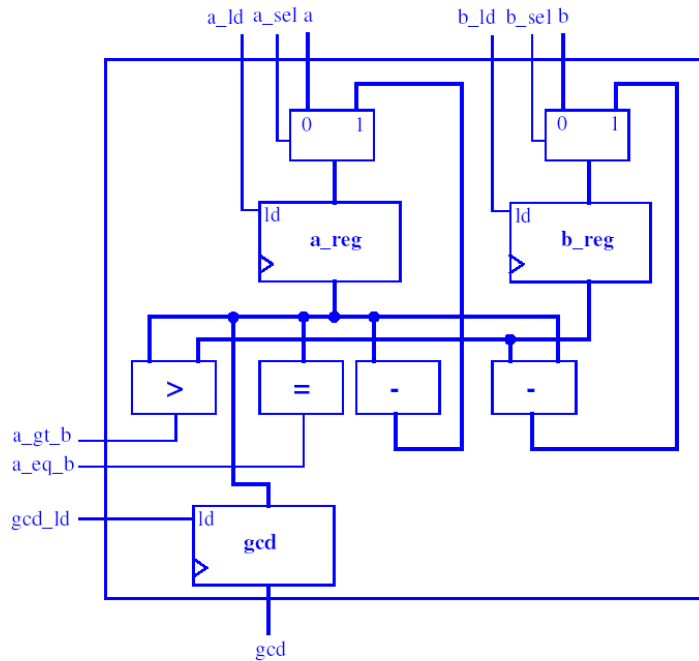


5.25 Use the RTL design method shown in Table 5.1 to convert the high-level state machine you created in Exercise 5.24 to a controller and a datapath. Design the datapath to structure, but design the controller to the point of an FSM only.

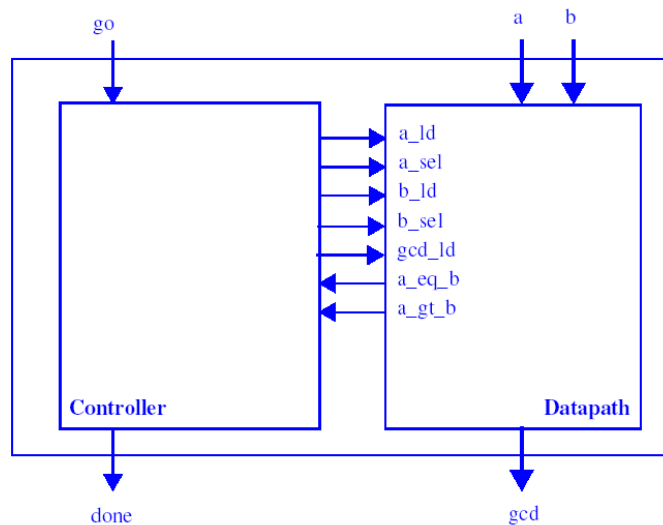
Step 1 - Capture a high-level state machine

The high-level state machine was developed in Exercise 5.24.

Step 2 - Create a datapath



Step 3 - Connect the datapath to a controller



Continued on next page

Problem 5.25 continued

Step 4 - Derive the controller's FSM

Inputs: go, done, a_gt_b, a_eq_b (bit)

Outputs: done, a_ld, a_sel, b_ld, b_sel, gcd_ld (bit)

