

6.20 Compare the logic size (as number of gate-inputs) and the delay (as number of gate delays) of a minimal bit width state encoding and an output encoding for laser-based distance measurer FSM shown in Figure 5.20.

Minimal bit width encoding:

State encodings: S0: 000, S1: 001, S2: 010, S3: 011, S4: 100

Inputs					Outputs							
s2	s1	s0	B	S	n2	n1	n0	L	Dreg_clr	Dreg_ld	Dcnt_clr	Dcnt_cnt
0	0	0	x	x	0	0	1	0	1	0	0	0
0	0	1	0	x	0	0	1	0	0	0	1	0
0	0	1	1	x	0	1	0	0	0	0	1	0
0	1	0	x	x	0	1	1	1	0	0	0	0
0	1	1	x	0	0	1	1	0	0	0	0	1
0	1	1	x	1	1	0	0	0	0	0	0	1
1	0	0	x	x	0	0	1	0	0	1	0	0

$n2 = s1s0S$
 $n1 = s1's0B + s1s0' + s1s0S'$
 $n0 = s1's0' + s1's0B' + s1s0' + s1s0S'$
 $L = s1s0'$
 $Dreg_clr = s2's1's0'$
 $Dreg_ld = s2$
 $Dcnt_clr = s1's0$
 $Dcnt_cnt = s1s0$

Logic size: 37 gate inputs
Delay: 2 gate delays

Output encoding:

State encodings: S0: 01000, S1: 00010, S2: 10000, S3: 00001, S4: 00100

Inputs						Outputs										
s4	s3	s2	s1	s0	B	S	n4	n3	n2	n1	n0	L	Dreg_clr	Dreg_ld	Dcnt_clr	Dcnt_cnt
0	1	0	0	0	x	x	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	x	0	0	0	1	0	0	0	0	0	1
0	0	0	1	0	1	x	1	0	0	0	0	0	0	0	1	0
1	0	0	0	0	x	x	0	0	0	0	1	1	0	0	0	0
0	0	0	0	1	x	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	1	x	1	0	0	1	0	0	0	0	0	0	1
0	0	1	0	0	x	x	0	0	0	1	0	0	0	1	0	0

$n4 = s1'B$
 $n3 = 0$
 $n2 = s0S$
 $n1 = s3 + s1x' + s2$
 $n0 = s4 + s0S'$
 $L = s4$
 $Dreg_clr = s3$
 $Dreg_ld = s2$
 $Dcnt_clr = s1$
 $Dcnt_cnt = s0$

Logic size: 13 gate inputs
Delay: 2 gate delays