Individual Homework 4 -- EECS 270, Fall '09

Due Monday, Oct 12th @2:00pm.

Name: ________________________________ unique name: ____________________

You are to turn in this sheet as a cover page for your assignment. The rest of the assignment should be stapled to this page. See the website for details about where to turn in your assignment. This is an individual assignment; all of the work should be your own. Assignments that are unstapled, lack a cover sheet, or are difficult to read will lose at least 50% of the possible points and we may not grade them at all.

This assignment is worth about 1% of your grade in the class and is graded out of 30 points. Remember you may drop two assignments (individual or group)

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1. You are to design a circuit which outputs the current priority level of an alarm system as a 5-bit unsigned number. There are 5 inputs. The first is a 4 bit unsigned value (CI[3:0]) which indicates the "old" priority level of the alarm system. The other 4 inputs (A, B, C and D) indicate what adjustments need to be made in the priority level. If "A" is high the output priority level should be 8 higher than the old value. If "B" is high and "A" is low the current level should be 4 higher than the old level. If "C" is high while "A" and "B" are low, the current level should be 2 higher than the old level. If "D" is high and A, B, and C are all low, the current level should be 1 higher than the old level. If none of the inputs A-D are high, the output should simply be the old level. You may freely tie inputs to Vcc or Ground. You may use any of the following:

   - 2-input AND gates, 2-input OR gates, 2-input XOR gates, NOT gates
   - 4-bit adders with carry-in and carry-out.
   - 8 to 3 encoders
   - 8 to 3 priority encoders with output enable
   - 3 to 8 decoders
   - 2 to 1 MUXes.

   You are to solve this with 5 or fewer devices. Be careful to *clearly* label devices, inputs and outputs. **[5]**

2. Draw the state transition diagram associated with figure 3.90 **[5]**
3. Draw the state transition diagram associated with figure 3.47 assuming: **[5]**
   - n1=b+s0
   - n0=b*s0+!s1*!b
   - x=s1
4. 3.47 **[3]**
5. 3.44 using a Moore machine. **[6]** (See example below. Notice that Y is delayed by 1 cycle because this is a Moore machine)
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X: 1010000100001110101001111
Y: 0001111100000111110111100
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6. Draw a Moore-type state transition diagram (not the circuit) for the following problem. Say we have two inputs, A and B, and one output, X. X should be high iff either the last 3 values of "A" were "111" or the last 3 values of "B" were 101. **[6]**
```
A: 0110000111000111100
B: 1001010000101001111
X: 0000001000100100110
```