EECS 270 Midterm *Exam Review*

Reminders:

- Our midterm exam is this Friday 10am-noon in our regular classroom. The exam is in 2 parts.
  - About 20 points will be closed book and you'll start there. Once you turn it in you'll get the open book part.
    - Expect questions like "draw the gates for an SR-latch with enable" or "draw the gates for a MUX", number representation (2's complement, different bases, etc.) basic timing/delay, and latch/flip-flop behavior.
  - The other ~80 points are open book and open notes.
- Everything other than *state* minimization is on the exam.
  - Includes labs 1-4.
- GA3 is due Thursday.
  - I've posted a template on the website which may be useful.
  - I've added a clarification about the problem on Piazza.
  - It's a lot of work.
- Next week:
  - No lab (including open lab), office hours etc. on Saturday, Sunday, or Monday.
    - Everyone gets a break (well, staff has to grade, but still).
  - Open lab and office hours as normal on Tuesday and beyond.
  - On Wednesday we have an individual homework due. It is posted.
  - On Friday the group homework is due and we have a quiz.
  - The group HW will be posted by Friday night.

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Friday May 26		**Midterm exam (in class)**	
Monday May 29	5	**Memorial Day--no class**	
Wednesday May 31		Memories and Datapath	HW4
Friday Jun 02		Datapath and transistors	Quiz3/GA4
Monday Jun 05	6	Transistors and faster adders	HW5
Wednesday Jun 07		Review CLA, Bus-based datapath design	GA5
Friday Jun 09		Bus-based datapath design;	Quiz4
Monday Jun 12	7	Mealy machines and QM minimization	HW6
Wednesday Jun 14		QM example, Mealy machines, errors	GA6
Friday Jun 16		Yet more Mealy, How logic is built	Quiz 5
Monday Jun 19	8	Class overview and practice problems.	
Thursday Jun 22		Final Exam, 4-6pm	

1. Using no more than five 2-input NAND gates and nothing else, design a MUX gate. You may freely use "0" and "1" as inputs. **[5 points]**

2. Convert the values as indicated: **[5 points, -1 per wrong or blank answer]**

   a) 23_{10} into 7-bit 2's complement _____

   b) -3_{10} into 4-bit 2's complement _____

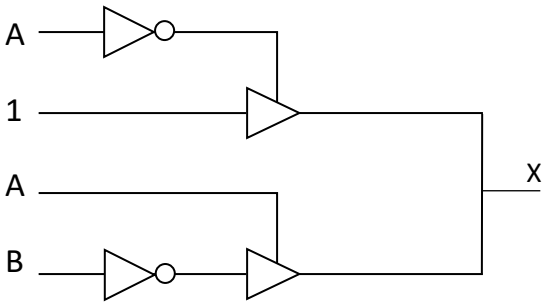
   c) 10001 from 5-bit 2's complement to decimal _____

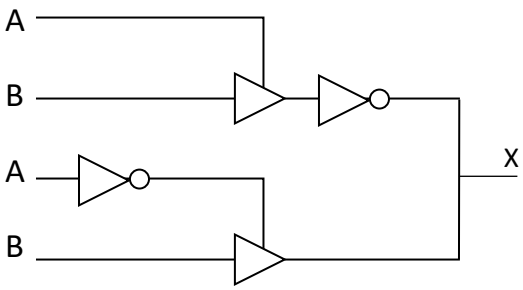
   d) -1_{10} into 4-bit 2's complement _____

   e) -4_{10} into 5-bit signed-magnitude _____

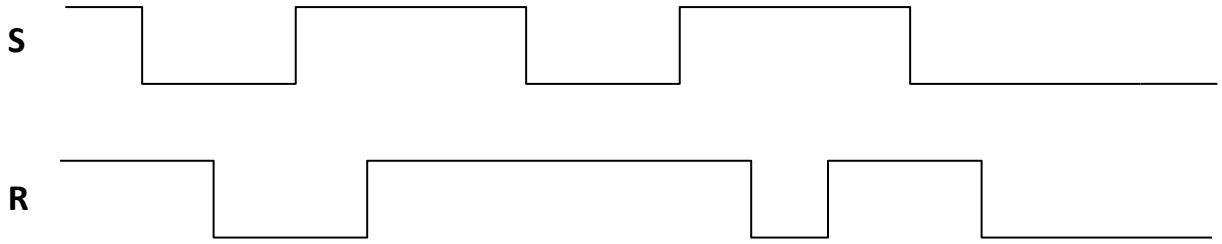
   f) 7.125_{10} into base 4 _____

3. Write a truth table for each circuit. For each case label it as "0", "1", "HiZ" or "???" (that last is if the value isn't known to be any of the other three). **[2 questions, 4 points each, 8 points total]**





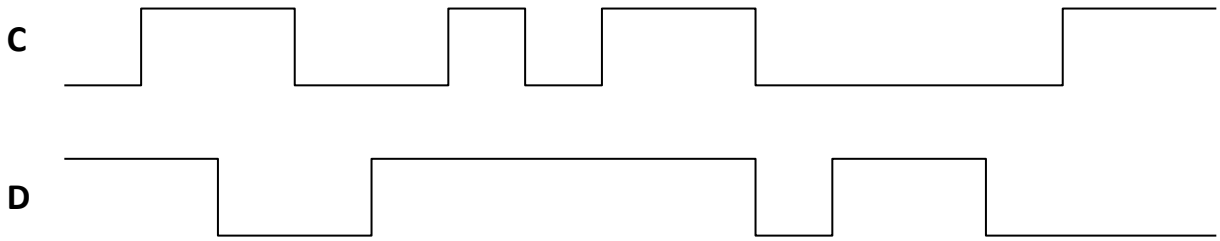
4. Functionality of latches and flip-flops
    a. Show the values of Q and QN for an SR latch with the following inputs. Leave blank any value you don't know. **[6]**



Q

QN

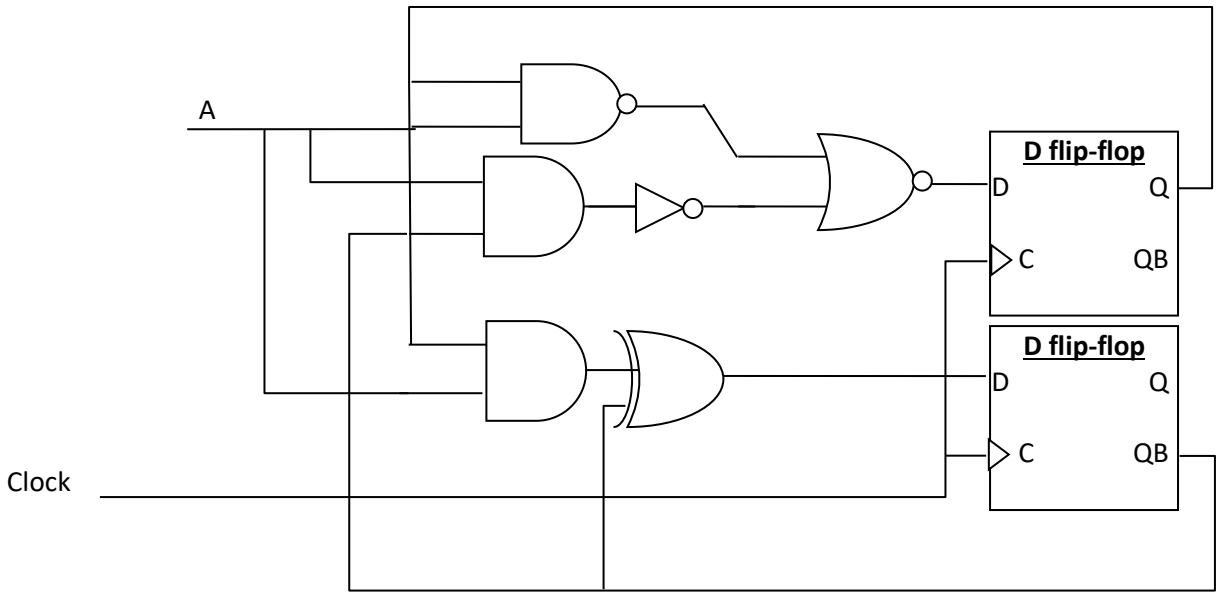
    b. Show the value of the output of a D-flip-flop given the following input. You should assume the initial value of Q is unknown. Leave blank any value you don't know. **[4]**



5. Design a *circuit* which has a single output input A[1:0] X that goes high only if the last 2 inputs (sampled on the rising edge of a clock input) were 3 and then 1. All combinational logic should be in minimal sum-of-products form.

	Min	Max
OR/AND	3ns	5ns
NOR/NAND	2ns	4ns
NOT	1ns	2ns
XOR	3ns	9ns

DFF:		**Min**	**Max**
	Clock to Q	2ns	3ns
	Set-up time	7 ns	
	Hold time	6 ns	



6. Assuming the input A ***always*** arrives 2ns after the rising edge of the clock, answer the following questions. **[12 points]**
   a) Add inverter pairs as needed to ensure that there are no hold time violations. Add as few pairs as possible. *If there is more than one way to add as few as possible, add them in a way that minimizes the period this can be clocked at.* **[6]**

   b) What is the lowest clock period that could be safely used to clock this circuit (including changes you made above)? Clearly show your work. **[6]**

7. ***<u>This question is quite hard!></u>***
   You are doing design work on an old circuit board and have two outputs you must generate based on 6 bits of input (A[2:0] and B[2:0], both treated as unsigned numbers). The following devices are available on the circuit board (***<u>only</u> one of each***):
   - a 3 to 8 decoder
   - a 6 to 3 MUX.
   - a 2 to 1 MUX
   - a 8 to 3 priority encoder
   - a 3-bit unsigned comparator. Outputs are LT, EQ, and GT
   - a 4-input OR gate
   - an inverter.

   You wish to use these devices to generate the following outputs:

   - **X** is 1 if A is greater than B or if B is 6 or 7. Otherwise X is 0.
   - **Y** is 1 if A is prime (2,3,5,7). Otherwise Y is a 0.

   Find a circuit that meets the design restrictions. You have free access to constants (zeros and ones). Be clear with your labeling of inputs, outputs and devices. If you can't do both X and Y, solve one for partial credit. **[15]**