

EECS 270 Class Schedule: Fall 2009

#	Date	Topic	Reading	Labs due	Homework
1	Wednesday, September 09	Class intro, intro to basic logic & logic circuits, binary/hex, MUX	1, 2.4-2.6	(Tutorial)	
2	Monday, September 14	More on basic logic, combinational logic design	2.7, 2.8	Lab 1 prelab	
3	Wednesday, September 16	Delay, MSI devices (MUX, decoder, encoder, P. encoder, comparator, adder)	2.9, 2.10	(Due at end of lab period)	HW1 due
4	Monday, September 21	Verilog introduction, negative numbers and adders/subtractors	handouts	Lab 1, Lab 2 prelab	GA 1 due
5	Wednesday, September 23	Logic practice and combinational review (w/ focus on number apps)	2.4-2.10, handout		
6	Monday, September 28	Latches and Flip-flops	3.1-3.2	Lab 2, Lab 3 prelab	HW2 due
7	Wednesday, September 30	More latches and flip-flops, FSM	3.2-3.3		
8	Monday, October 05	More FSM, Seq. Verilog	3.3, handout	Lab 3 part 1	HW3 due
9	Wednesday, October 07	Yet more FSM and FSM controller design	3.3, 3.4		
10	Monday, October 12	Even more FSM, non-ideal issues	3.4, 3.5	Lab 3 part 2, Lab 4 prelab	GA2 due
11	Wednesday, October 14	Exam 1 review, covers lec 1-9 (Exam 1: 7-9pm)	----		
	Monday, October 19	Study Break -- NO CLASS	----	Lab 4	
12	Wednesday, October 21	Timing (delay, set-up and hold, glitches), determining clock freq.	3.5, (5.4), handout	(Due by Friday)	
13	Monday, October 26	MSI/datapath: Registers, Adders and Shifters (oh my)	4.1-4.4	Lab 5 prelab	HW4 due
14	Wednesday, October 28	MSI/datapath: Comparators, Counters, Array multiplier	4.5-4.7		
15	Monday, November 02	MSI/datapath: ALUs, Register files, memories	4.8-4.10, handout	Lab 5	GA3 due
16	Wednesday, November 04	Digital design	5		
17	Monday, November 09	Digital design	5	Lab 6 prelab	HW5 due
18	Wednesday, November 11	Combinational logic optimization (Basic notions, start on Kmaps)	6.1-6.2		
19	Monday, November 16	Combinational logic optimization (More Kmap)	6.2	Lab 6	
20	Wednesday, November 18	Combinational logic optimization (Q-M, what it means to optimize)	Handout		HW6 due
21	Monday, November 23	Exam 2 review, covers lec 1-19 (Exam 2: 7-9pm)	----	Lab 7 pre-lab	
22	Wednesday, November 25	Sequential logic optimization (State Reduction)	6.3	(Due by Wednesday)	
23	Monday, November 30	Sequential logic optimization (State encoding, Moore vs. Mealy)	6.3	Lab 7 part 1	HW7 due
24	Wednesday, December 02	Optimization practice/review	6.1-6.3, handout		
25	Monday, December 07	Faster adders (and maybe multipliers)	6.4	Lab 7 part 2	GA4 due
26	Wednesday, December 09	CMOS design	2.1-2.4	(Due at end of lab period)	
27	Monday, December 14	TBD/catchup	TBD	No lab	HW8 due
	Wednesday, December 16	Final exam (10:30am-12:30pm)			

Notes:

- * All lab assignments are due in the first 30 minutes of lab unless otherwise noted.
- * Postlabs are due at the same time as the last part of the inlab
- * HW is individual homework, GA is a Group Assignment
- * HW & GA are due by 2pm in box.