EECS 270 *Midterm Exam*

Spring 2011

Name: KEY unique name: KEY

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

Scores:

Page #	**Points**
2	/15
3	/10
4	/6
5	/12
6	/10
7	/15
8	/12
9	/8
10	/12
Total	**/100**

NOTES:

1. Open book and Open notes
2. There are 10 pages total. Count them to be sure you have them all.
3. Calculators are allowed, but no PDAs, Portables, Cell phones, etc.
4. This exam is fairly long: *don't spend too much time on any one problem*.
5. You have about 120 minutes for the exam.
6. Some questions may be more difficult than others. You may want to skip around.
7. **Be sure to show work and explain what you've done when asked to do so.** Even if work isn't requested it is a good idea to provide your work as it will help with partial credit.

Short Answer/Fill in the blank

1. Fill in each blank or circle the best answer.
[15 points, -2 per wrong or blank answer, min 0]

a. If you were going to build a 1-bit equals comparator with a single gate, you'd use a XNOR gate.

b. A clock period of 10ns corresponds to a frequency of 100 MHz.

c. The *canonical* product-of-sums representation of (A+B')*(A+C') is

$(A+\bar{B}+c)\cdot(A+B+\bar{c})\cdot(A+\bar{B}+\bar{c})$

d. 7 is the largest value that can be represented by a 4-bit 2's complement number. Provide your answer in decimal.

e. The 6-bit 2's complement number representation of -11 is 110101.

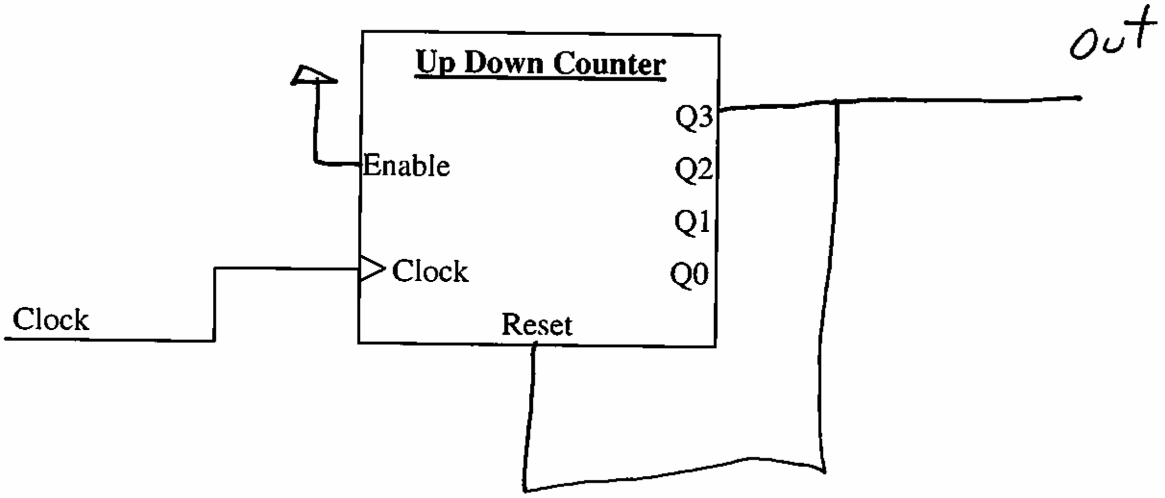
f. 10001, when treated as a 5-bit signed-magnitude number, has a decimal representation of -1.

g. 4.375 would be represented in binary as: 100.011

h. DRAM is typically ***faster*** / [✓ ***slower***] than SRAM.

i. The statement F=a'b+b'c consists of 3 variables and 4 unique literals. If it were rewritten to be in canonical sum-of-products form it would have 4 minterms.

2. Using a 4-bit up/down counter with enable and reset (shown below) and as few standard gates as possible, design a circuit that outputs a 1 every 9th clock period. Be sure all your inputs are driven by something (you may freely use ground and Vcc). Partial credit given for working but inefficient designs. **[5 points]**

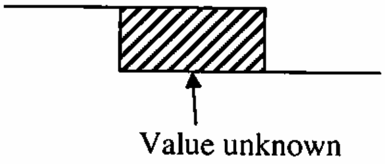


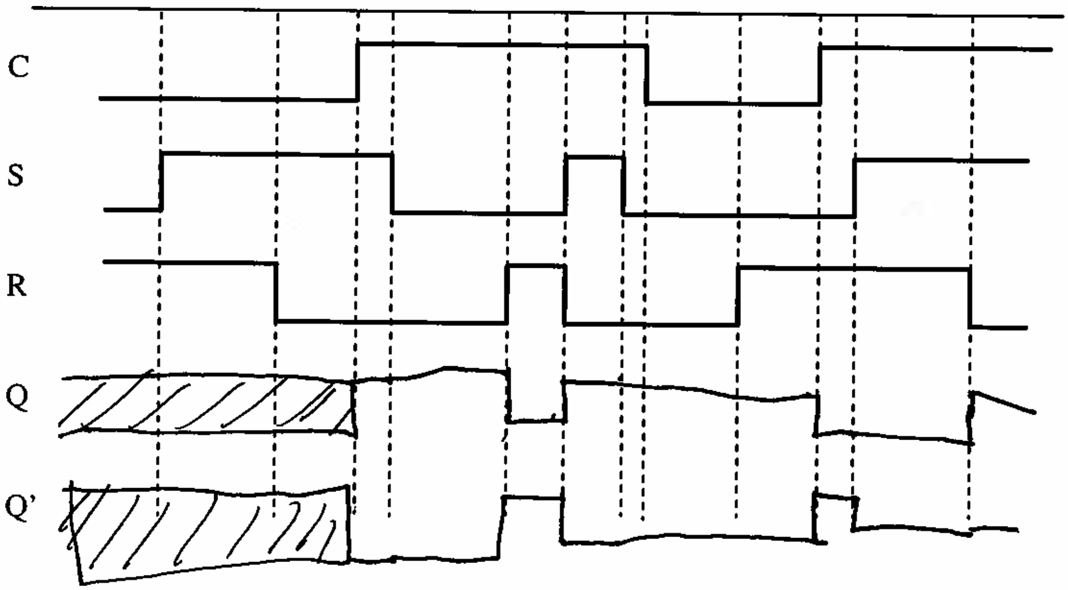
3. Using the rules of logic, convert (A*B)'*(A'*C) into a *minimal* sum-of-products form. Provide the name of the rule used for each step. **[5 points]**

No ans. provided.

4. Complete the following timing diagram for an SR-latch with enable. **[6 points]**

If the value is unknown (or oscillating) at some point, clearly indicate that with hashes (like this)



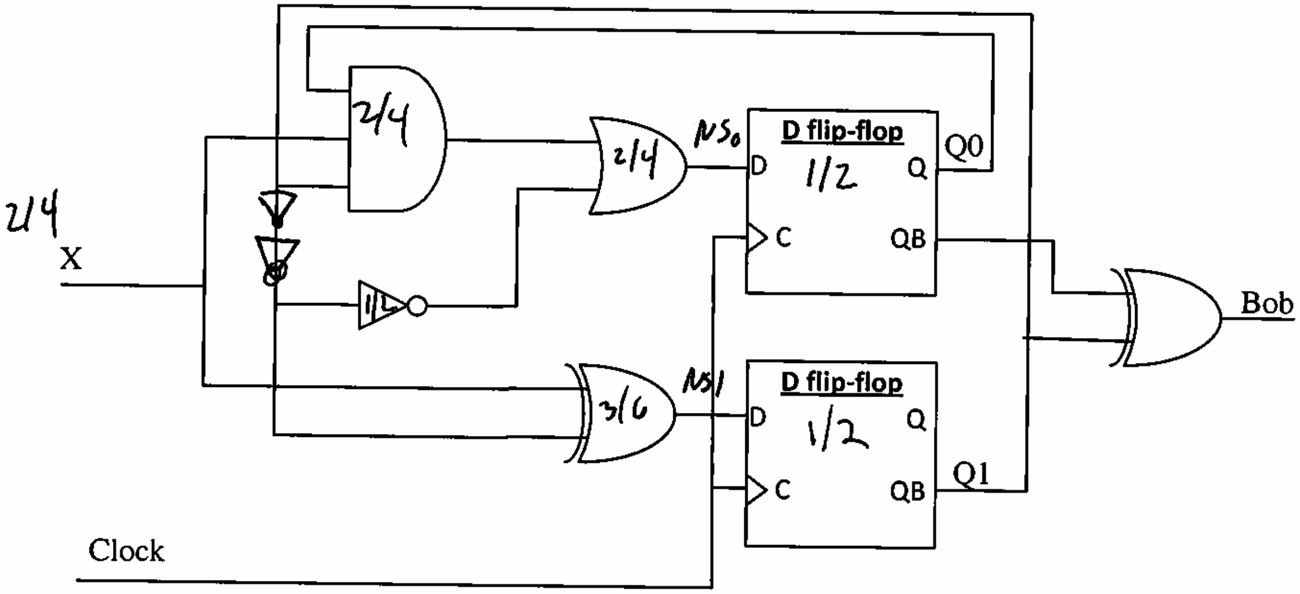


Longer answer

1) Say you have the following values associated with the process you are using:

DFF:		Min	Max
	Clock to Q	1ns	2ns
	Set-up time	4ns	
	Hold time	5ns	
OR/AND	(2 or 3 input)	2ns	4ns
NOT		1ns	2ns
XOR		3ns	6ns
NAND		1ns	3ns

The input ("X") can change as early as 2ns after the rising edge of the clock and as late as 4ns after the rising edge of the clock.



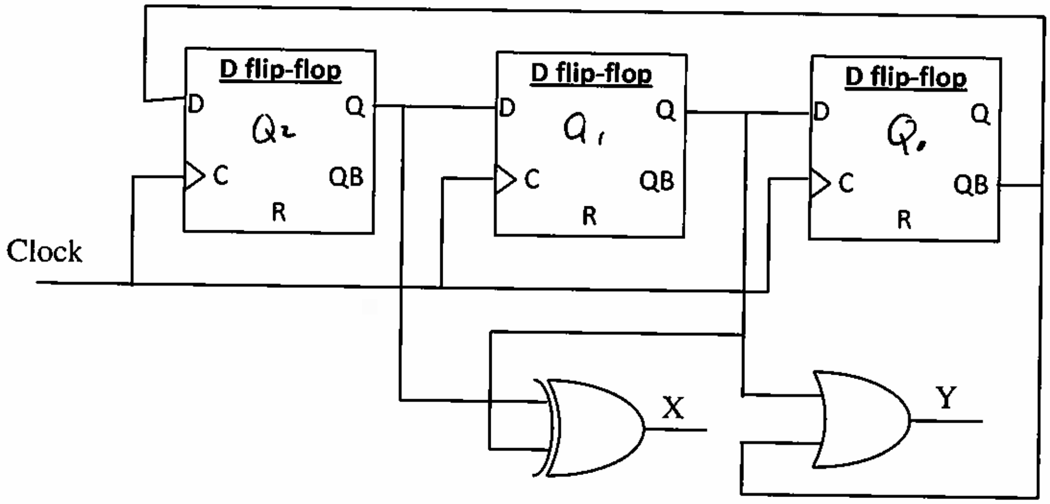
a. Add inverter pairs (as needed) to insure the hold time requirements will be met. You should add them in a way that has the least impact on the worst-case delay (as a first priority) and which keeps the number of inverter pairs needed to a minimum (as a second priority). **[5 points]**

b. After you've made your changes in part a, compute the maximum frequency at which this device can be safely clocked. Clearly show how you got your answer. **[7 points]**

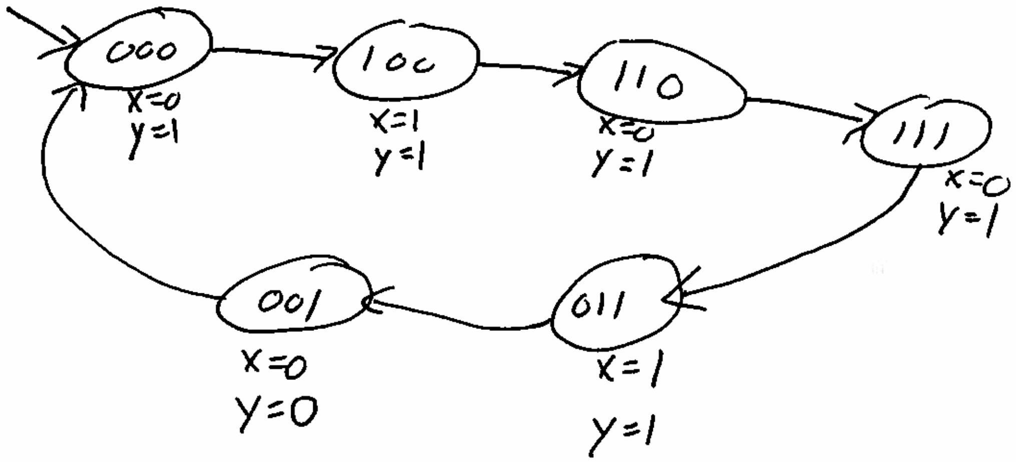
	Clock to Q	CL Delay	Setup	~~Q₀ to NS₀~~
Q₀ to NS₀	2 ns	10 ns	4 ns	
~~X to NS₁~~ Q₀ to NS₁	Clock to ~~X~~Q	CL Delay	Setup	
	~~4~~2 ns	10 ns	4 ns	

16 ns → 62.5 MHz

2) Draw the state-transition diagram that describes the following state-machine. Show your work. You may assume that the minimum clock to Q delay is greater than the hold time. Assume the initial state is when all the flip-flops have a value of 0. Your state transition diagram should only include those states that can ever be reached when you start at the initial state. **[10 points]**

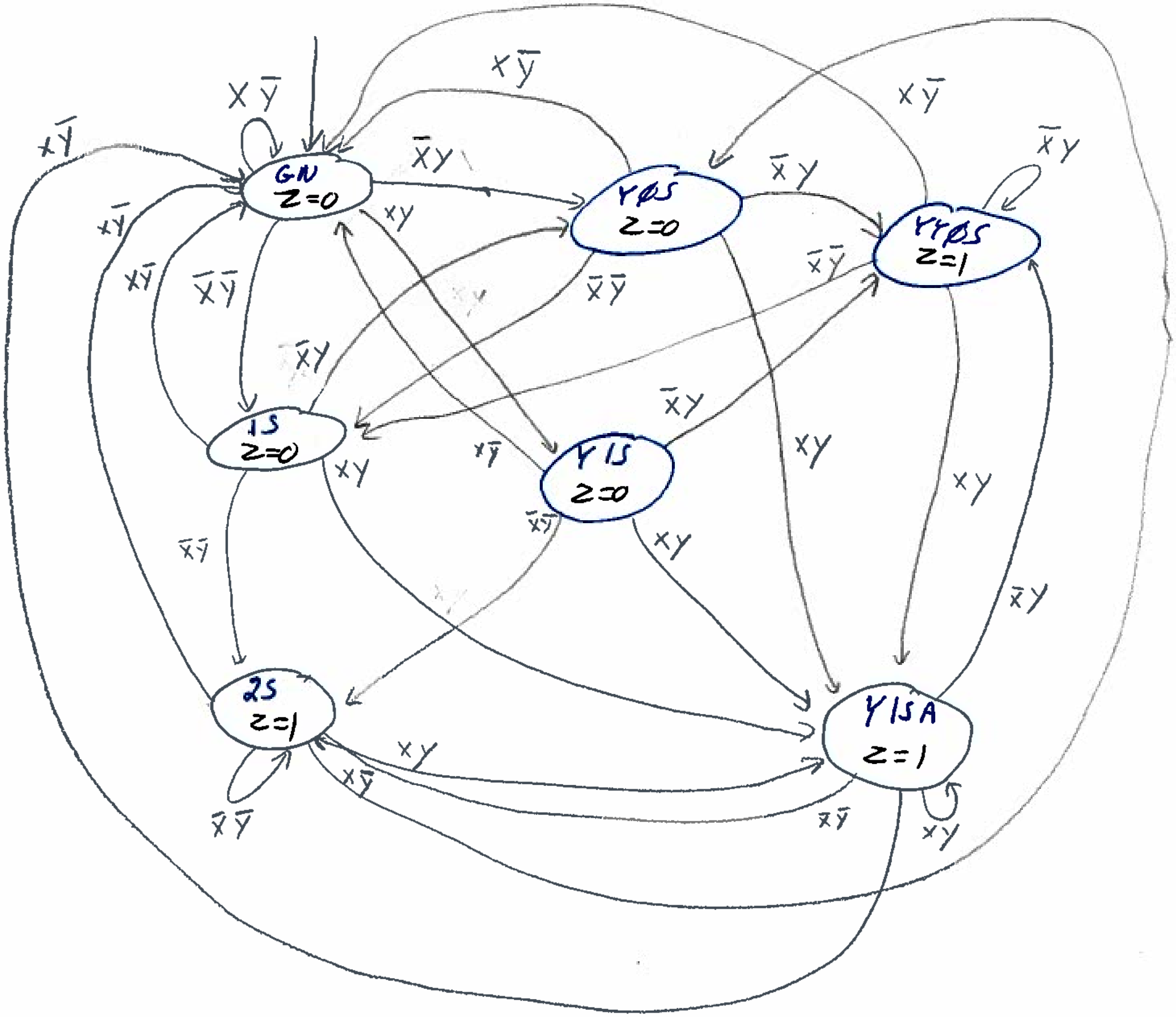


$Y = Q_1 + \overline{Q_0}$

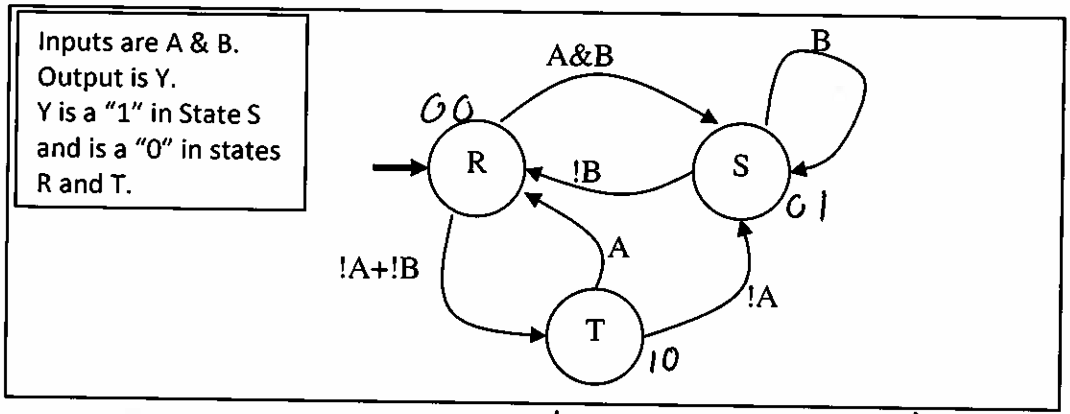


3) Design a state-transition diagram for a state machine with two inputs, X and Y, and one output "Z". The output should be a "1" if either X and Y were both the same for the last two cycles or if the last two values of Y were "11". To receive points, your answer must have no more than 12 states.

[**15 points**; 12 points for a correct answer; 3 extra for a correct *and* minimal-state answer]



4) For this problem, assign state bits S[1:0] as 00 for state R, 01 for state S, and 10 for state T. <u>Using K-maps</u>, find ***the minimal*** <u>*sum-of-products*</u> for next state (NS[1:0]) and the outputs (Y and Z). You are to assume that you will never reach the state S[1:0]=11, so you don't care what happens in that case. You must show your work to get <u>any</u> credit! **[12 points]**


Inputs are A & B.
Output is Y.
Y is a "1" in State S and is a "0" in states R and T.

S1	S0	A	B	NS1	NS0
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	D.C	
1	1	0	1	D C	
1	1	1	0	D.C	
1	1	1	1	D.C	

NS1

AB \ S1 S0	00	01	11	10
00	1	0	d	0
01	1	0	d	0
11	0	0	d	0
10	1	d	d	0

NS0

AB \ S1 S0	00	01	11	10
00			d	1
01		1	d	1
11	1	1	d	
10			d	

S0 \ S1	0	1
0	0	0
1	1	d

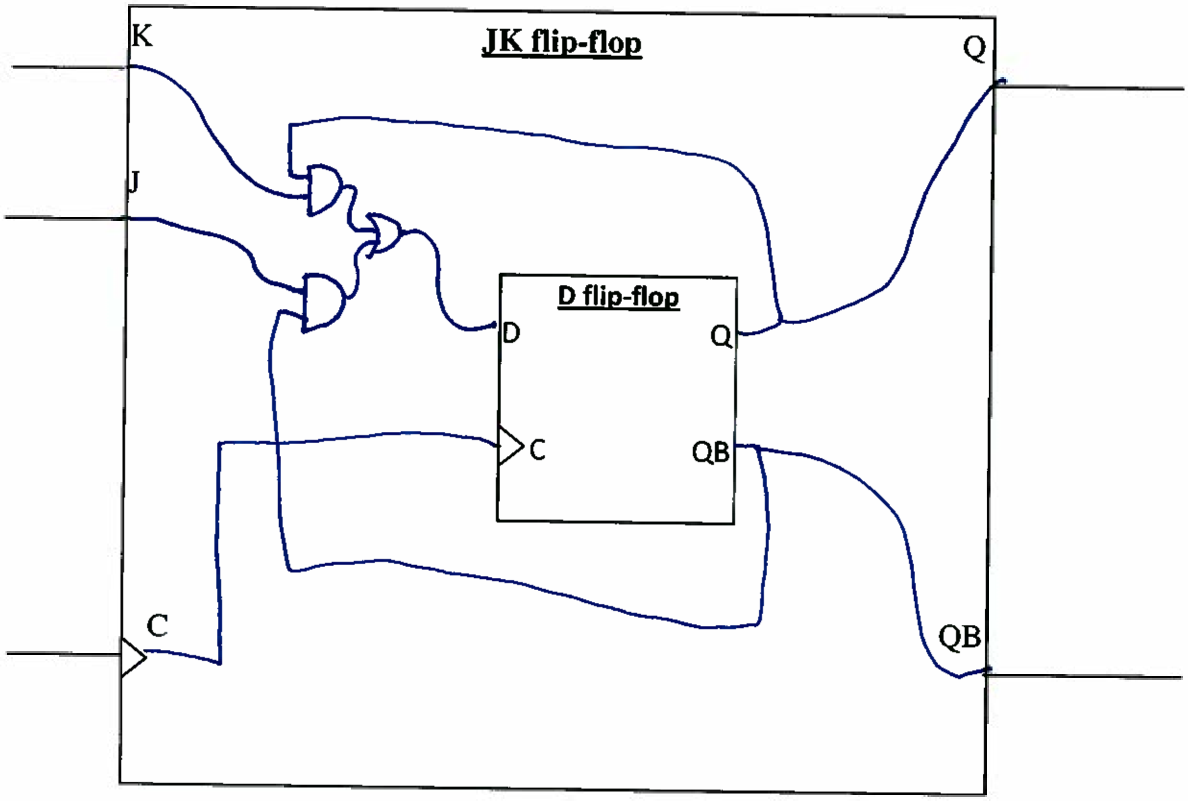
NS1= $\overline{S1}\cdot\overline{S0}\cdot\overline{A} + \overline{S1}\cdot\overline{S0}\cdot\overline{B}$

NS0= $S1\overline{A} + S0B + \overline{S1}AB$

Y= $S0$

5) Build a JK flip-flop out of a D flip-flop that has no enable or reset as well as standard gates. **[8 points]**

- The combination J = 1, K = 0 is a command to set the flip-flop;
- The combination J = 0, K = 1 is a command to reset the flip-flop;
- The combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value.
- The combination J = K = 0 is a command to hold the current value.



D:

J	K	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q \ JK	00	01	11	10
0			1	1
1	1			1

$$D = J \cdot \bar{Q} + \bar{K} \cdot Q$$

6) Consider the function F= $\Sigma_{wxyz}(0,1,3,8,12,13,14) + d(15)$.

a) List all the prime implicants (each implicant should be in the form of a product term) **[3 points]**

~~$wxy\bar{z}$~~

$wx, w\bar{y}\bar{z}, \bar{x}\bar{y}\bar{z}, \bar{w}\bar{x}\bar{y}, \bar{w}\bar{x}z$

b) List all the distinguished ones (each distinguished one should be in the form of a product term) **[2 points]** 3, 13, 14

$\bar{w}\bar{x}yz, wx\bar{y}z, wxy\bar{z}$

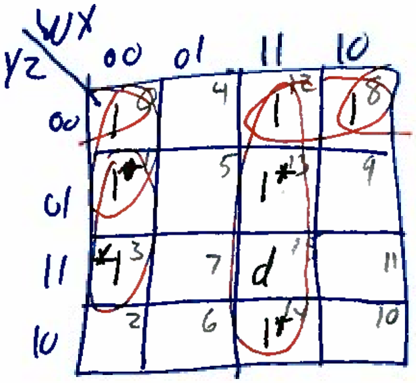
c) List all of the essential prime implicants (again each implicant should be in the form of a product term) **[3 points]**

$wx,$

$\bar{w}\bar{x}z$

d) Write a minimal sum-of-products equation for this function. **[4 points]**

$wx + w\bar{y}\bar{z} + \bar{w}\bar{x}z$



yz \ wx	00	01	11	10
00	1 0	4	1 12	1 8
01	1* 1	5	1* 13	9
11	*1 3	7	d 15	11
10	2	6	1* 14	10