EECS 270 *Midterm 1 Exam* Closed book portion

Spring 2022

Name: Key unique name: Key

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

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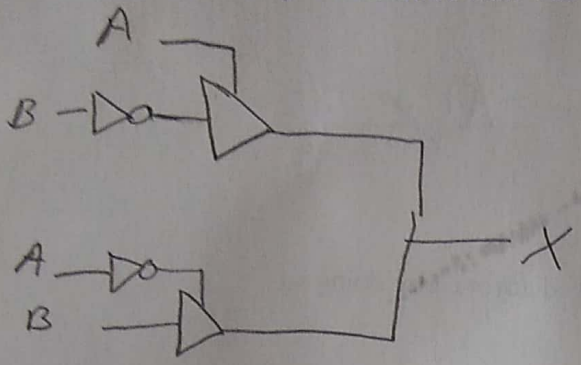
NOTES:

1. ***This part of the exam is closed everything. No calculators, books, notes, etc.***
2. Once you finish this part, turn it in and you'll be given the open book part. You won't be able to come back to this part.
3. There are 3 pages total. Count them to be sure you have them all.
4. You have about 120 minutes for the exam total. We'd suggest you not spend more than 25 minutes or so on this part.
5. In this document we use * for AND, + for OR, ! for NOT, and $\oplus$ for XOR.

1. Using only inverters and tri-state buffers, implement an XNOR gate with inputs A, B and an output X. You may use no more than 4 devices total. **[4 points]**



2. Fill in each blank. **[8 points, -1.5 per wrong or blank question, min 0]**

   a) The 5-bit 2's complement number representation of -4 is 11100.

   b) The range of representation for a 4-bit signed-magnitude number is from -7 to 7.

   c) The number 22.3_8 is 12.6 in base 16.

   d) If a clock has a frequency of 500MHz, it has a period of 2 ns

   e) The canonical sum-of-products representation of (A+B) is $AB + A\bar{B} + \bar{A}B$

   f) The canonical product-of-sums representation of !(A*B) is $\bar{A} + \bar{B}$

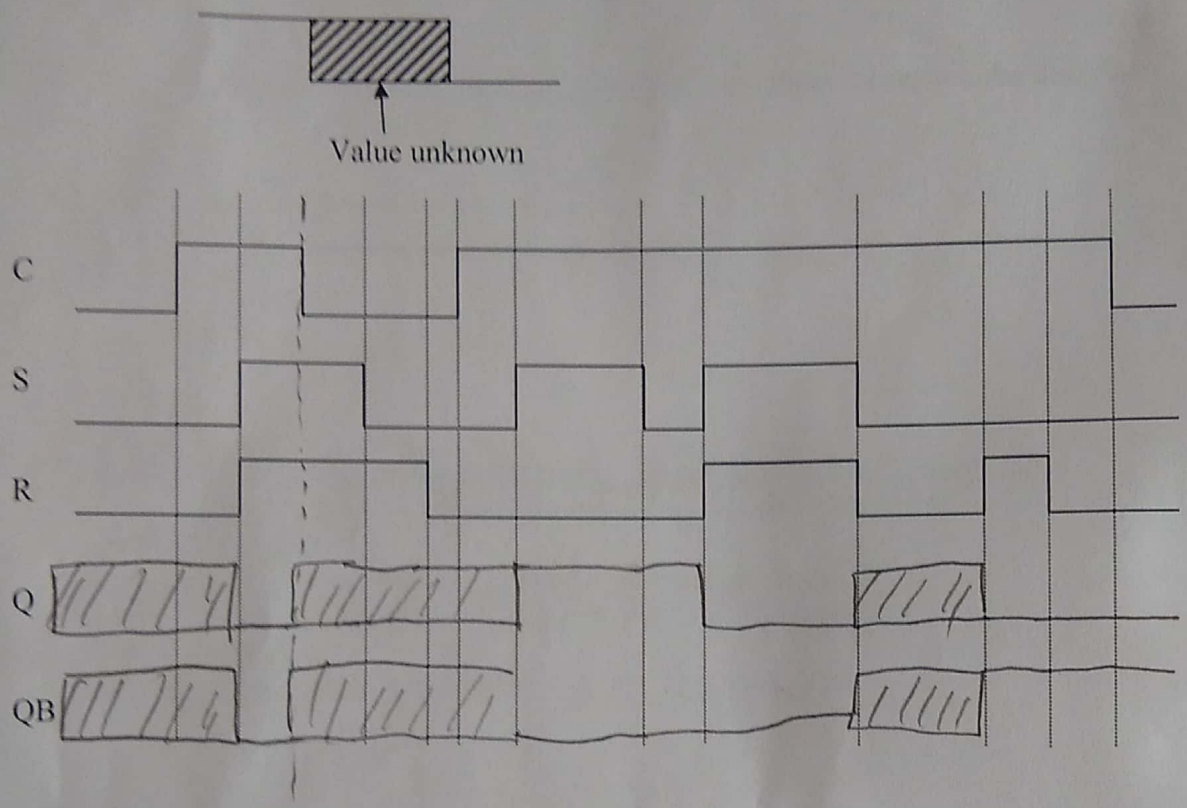
3. Prove some version of De Morgan's law by using perfect induction. **[3]**

$$\bar{a} \cdot \bar{b} = \overline{a+b}$$

a	b	$\bar{a} \cdot \bar{b}$	$\overline{a+b}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

4. Complete the following timing diagram for an SR-latch with enable. You may assume that the time scale is such that the gate delay is extremely small and your answer should not reflect those delays. Changes shown to be simultaneous are exactly simultaneous. **[5 points]**

If the value is unknown (or oscillating or metastable) at some point, clearly indicate that with hashes (like this)



EECS 270 *Midterm 1 Exam* Open book portion

Spring 2022

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NOTES:

1. ***This part of the exam is open books and open notes. You may not use any device capable of communication (cell phones, calculators with wireless, etc.)***
2. You have about 120 minutes for the exam total.
3. Some questions may be harder than others. Manage your time wisely.
4. Unnecessarily complex designs will likely not get full credit.
5. Be sure to show your work when asked.

1) Using the rules of logic, show that (!a+b*c)=(!a+b)*!(!c*a) or show it is false. You must show each step and clearly identify each rule used. **[5 points]**

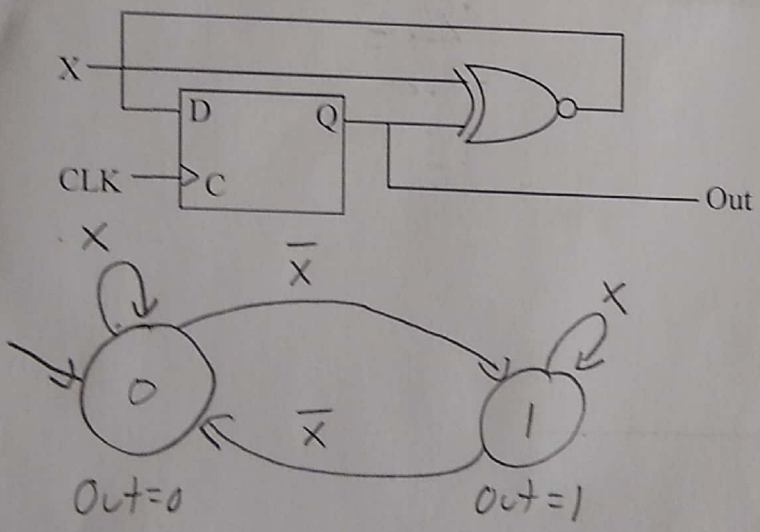
$\bar{a}+bc$ given

$(\bar{a}+b)(\bar{a}+c)$ distributive law

$(\bar{a}+b)(c+\bar{a})$ Commutative law

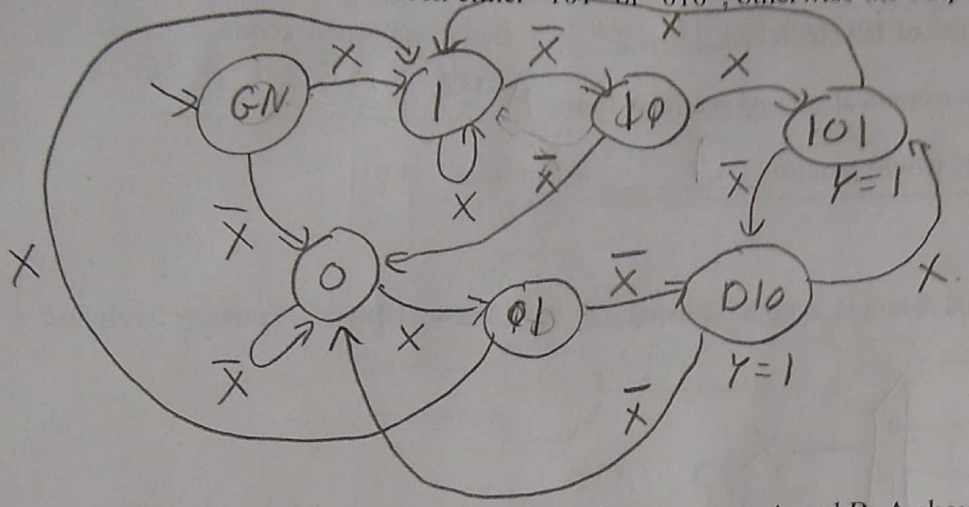
$(\bar{a}+b)(\overline{\bar{c}+a})$ De Morgan law

2) Draw a state transition diagram for the following state machine. The initial state is when the flip-flop has the value 0. **[5 points]**



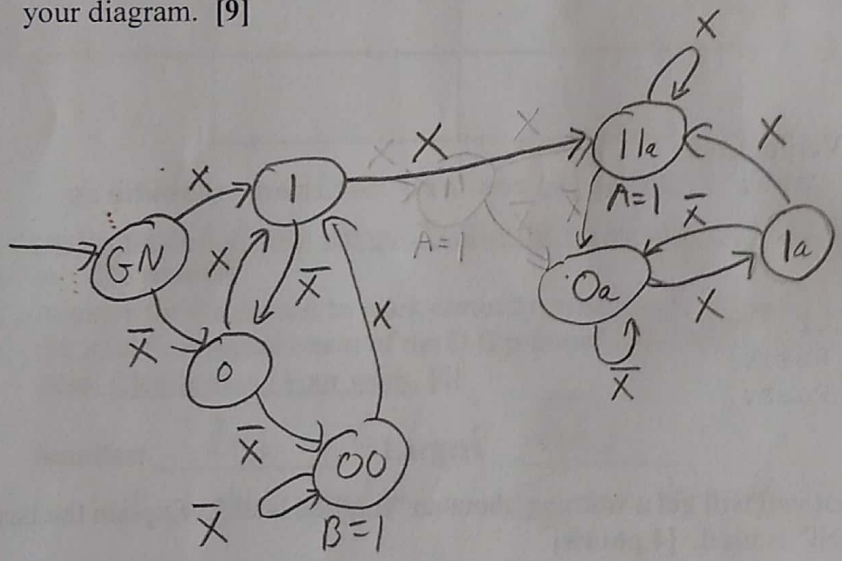
3) Design a state transition diagram for each of the following: **[15 points]**

a. The machine has one input X and one output, Y. The output is to go high if the most recent values of X has been either "101" or "010", otherwise the output is to be low. **[6]**



Y=0 unless shown

b. The machine has one input X and two outputs A and B. A should go high if the most recent values of X were "11". B should go high if the most recent values of X were "00" *and* X hasn't yet been "11" at any point (since reset). Note: reset is not an input—it shouldn't be in your diagram. **[9]**



A and B are zero unless shown

4) Fill-in-the-blank: **[5 points, -1.5 per wrong or blank question, min 0]**

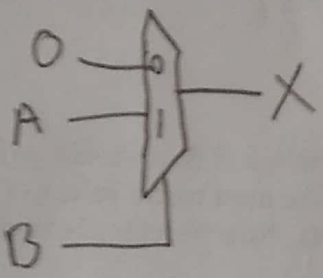
a. Write A⊕!B in canonical *product-of-sums* form: $(A+B)(A+\bar{B})$

b. If a clock has a period of 10kHz, it has 10,000 rising edges per second.

c. Write A*C+A*B in canonical *sum-of-products* form: $A\,BC + A\,\bar{B}C + A\,B\bar{C}$

d. A 6-bit 8-to-1 MUX would require 3 select lines.

5) Design an AND gate (inputs A and B, output X) using only a 1-bit 2-to-1 MUX. You may freely use 0s and 1s. **[4 points]**



6) Consider the following Verilog code:

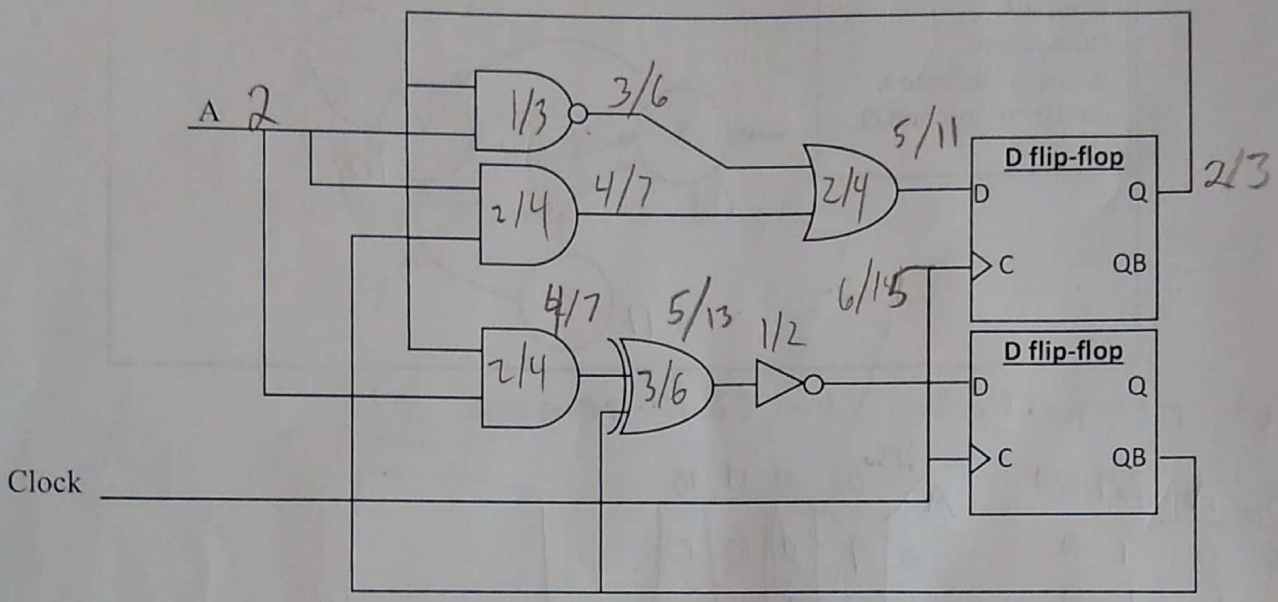
```
wire Trigger, Pass; //These wires are defined elsewhere
reg A, C;
always @* begin
      A = 1'b0;
      if (Trigger) begin
            A = Pass;
            C = Pass;
end
```

The above code compiles, but you will get a warning about an "implied latch". Explain the issue including why the word "latch" is used. **[4 points]**

It is possible to go through the code and not have a value assigned to C. So the tool will assume that it should use the old value of C. To do so, it will need to create a memory (latch). This was not the intended behavior

	Min	Max
OR/AND	2ns	4ns
NOR/NAND	1ns	3ns
NOT	1ns	2ns
XOR/XNOR	3ns	6ns

DFF:		Min	Max
	Clock to Q	2ns	3ns
	Set-up time	7 ns	
	Hold time	??? ns	



7) Assuming the input A *always* arrives 2ns after the rising edge of the clock, answer the following questions. **[10 points]**

- In order for this circuit to work correctly, what range of values that would be acceptable for the hold time *requirement* of the D flip-flops? Assume the only options range from 1ns to 20ns. Clearly show your work. **[4]**

Smallest 1ns **Largest** 5ns

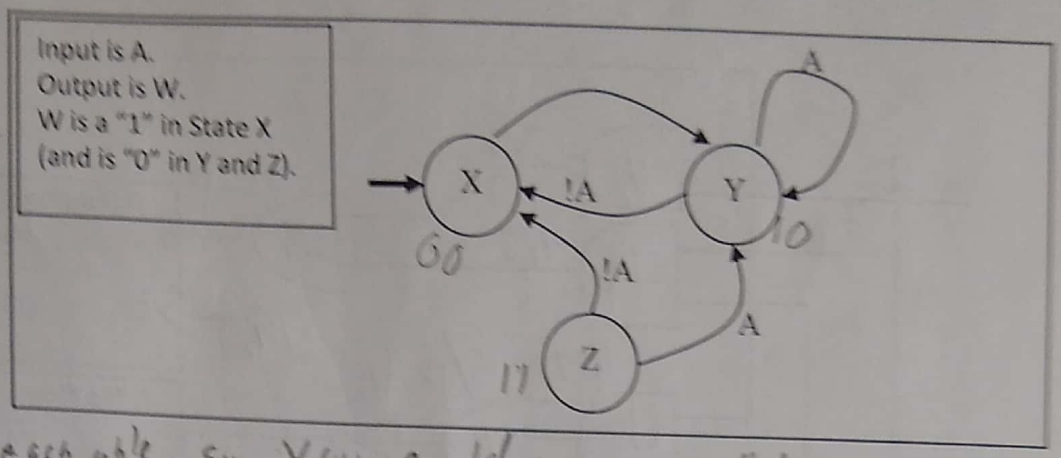
fastest path is 5ns to the top FF.

- What is the lowest clock period that could be safely used to clock this circuit? Clearly show your work. **[6]**

longest path is 15ns. setup is 7ns

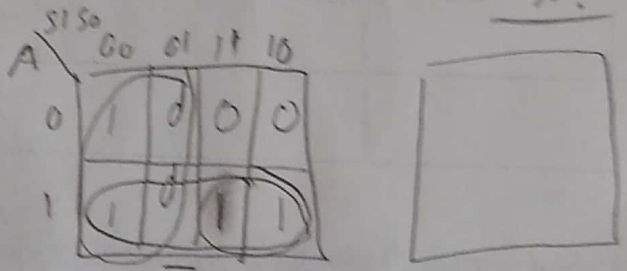
so 22ns

8) Design a state machine which implements the following state transition diagram. Assign state bits S[1:0] as 00 for state X, 10 for state Y, and 11 for state Z. You are to assume that you will never reach the state S[1:0]=10, so you don't care what happens in that case. You must show your work to get any credit! *You only need to compute the next state and output logic, you don't need to draw the gates or flip-flops!* Place your answer where shown, ***all answers must be in minimal sum-of-products form.*** **[12 points]**



Z not reachable, so you could remove it.

S_1	S_0	A	N1	N0
0	0	0	1	0
0	0	1	1	0
0	1	0	d	d
0	1	1	d	d
1	0	0	0	0
1	0	1	1	0
1	1	0	0	0
1	1	1	1	0



$N1 = \overline{S1} + A$

$N0 = 0$

$W = \overline{S1}$

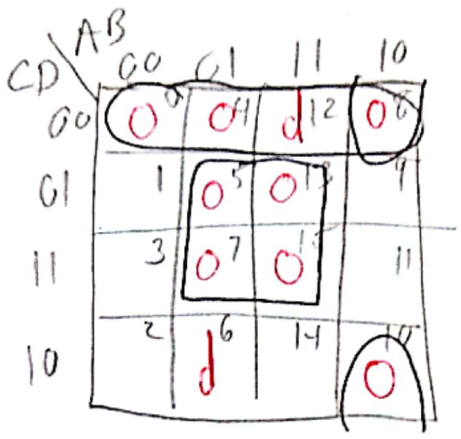
(Be sure all are in sum-of-products form!)

NS1= $\overline{S1} + A$

NS0= 0

W= $\overline{S1}$

9) Find the minimal *product-of-sums* for $\sum_{ABCD}(1,2,3,9,11,14)+d(6,12)$. Clearly show your work. **[10 points]**



$$(C+D)(\bar{B}+\bar{D})(\bar{A}+B+D)$$

10) Using the devices provided and no more than 2 standard gates (with any number of inputs) design a state machine that has a single input, A, and single output X. X should go high if the last values of A were either 10 or 111. On the rising edge of clock, the shift-in value will go to Q4 and the other values will shift down (so Q3 gets the old value of Q4 etc.) on the rising edge of clock. [10 points]

10 = Q4=0
Q3=1

111 = Q4, Q3, Q2=1