EECS 270 *Midterm Exam* Closed book portion

Spring 2023

Name: Key unique name: Key

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

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NOTES:

1. ***This part of the exam is closed everything. No calculators, books, notes, etc.***
2. Once you finish this part, turn it in and you'll be given the open book part. You won't be able to come back to this part.
3. There are 4 pages total
4. You have about 120 minutes for the exam total. We'd suggest you not spend more than 15 minutes or so on this part.
5. In this document we use * for AND, + for OR, ! for NOT, and ⊕ for XOR.

00111 → 11000 → 11001
−16 8 4 2 1

1. Fill in each blank or circle the best answer. **[7 points, -1.5 per wrong or blank question, min 0]**

   a) The 5-bit 2's complement number representation of -7 is 11001.

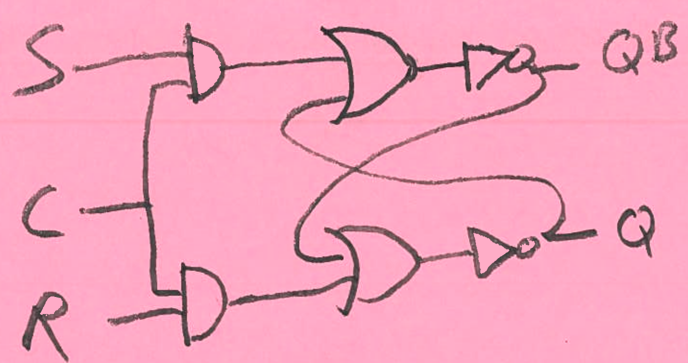
   b) The range of representation for a 6-bit two's complement number is from -32 to 31.

   c) The canonical product-of-sums representation of (AB+!A!B) is $(\bar{A}+B)(A+\bar{B})$

   d) The frequency of a 20ns clock is 0.05 GHz.

   e) With a D-flip-flop, there is a short period after the rising edge of the clock where the D input must remain constant or the flip-flop may not behave correctly. That short time is called the hold time

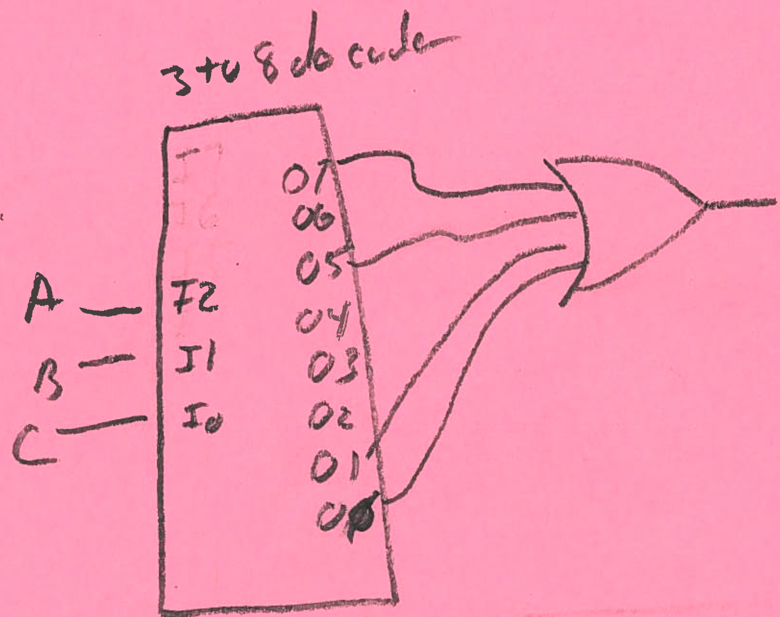
2. Draw the gates needed to implement an SR latch with enable using only AND, OR and NOT gates (no bubbles, NOR gates, or NAND gates). **[3 points]**



A	B	
0	0	1
0	1	0
1	0	0
1	1	1

3. Using only a decoder and an OR gate, draw a circuit which implements the following: !(A+B)+A*C
Be sure things are clearly labeled. **[5 points]**

$\bar{A} \cdot \bar{B} + A \cdot C$



A B C	
0 0 0	1
0 0 1	1
0 1 0	
0 1 1	
1 0 0	
1 0 1	1
1 1 0	
1 1 1	1

0, 1, 5, 7

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If you write anything here you want graded be sure to mention it on the page with the relevant problem

EECS 270 *Midterm Exam* Open book portion

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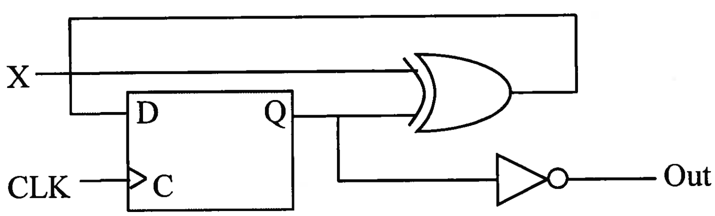
NOTES:

1. ***This part of the exam is open books and open notes. You may not use any device capable of communication (cell phones, calculators with wireless, etc.)***
2. You have about 120 minutes for the exam total.
3. Some questions may be harder than others. Manage your time wisely.
4. Unnecessarily complex designs will likely not get full credit.
5. Be sure to show your work when asked.

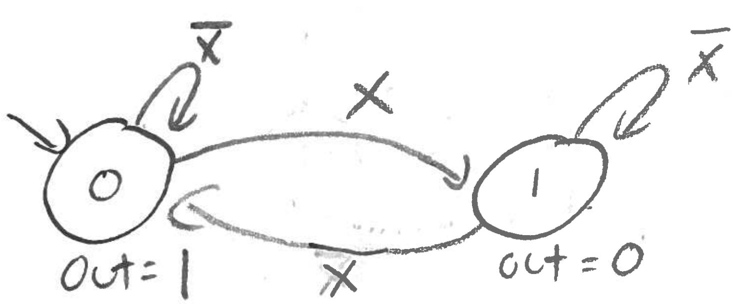
1. Using the *rules of logic*, convert !(A+!C)+(A*C) into a *minimal* sum-of-products form. Provide the name of the rule used for each step. **[5 points]**

$!(A+!C) + A\cdot C$	Given
$\bar{A}\cdot\bar{C} + AC$	Demorgan's
C	Combining.

2. Draw a state transition diagram for the following state machine. The initial state is when the flip-flop has the value 0. **[5 points]**



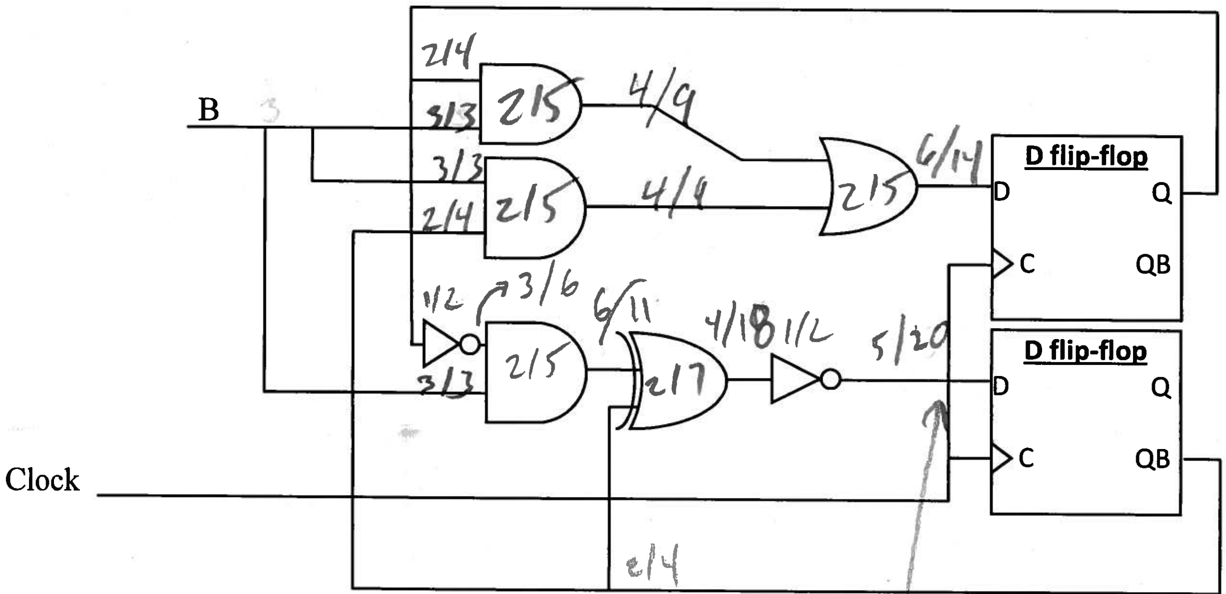
X	Q	D
0	0	0
0	1	1
1	0	1
1	1	0



3. Say you have the following values associated with the process you are using (notice the hold and set-up times are not specified). Assume you intend to clock this circuit at ~~50~~MHz. 30ns

Dff:	Min	Max
Clock to Q	2ns	4ns
Set-up time	?? ns	
Hold time	?? ns	

	Min	Max
OR/AND	2ns	5ns
NOT	1ns	2ns
XOR	2ns	7ns



Assuming the input B *always* arrives 3ns after the rising edge of the clock, answer the following questions. **[10 points]**

a) Assuming you want a reliable circuit, what is the highest value the flip-flop could have for a hold time? Clearly show your work. **[5]**

fastest value at D input can change after ↑ of Clock is 5ns

5 ns

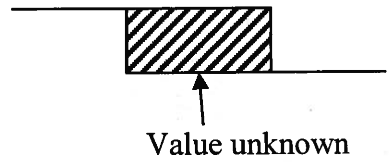
b) Assuming you want a reliable circuit, what is the highest value the flip-flop could have for a setup time? Clearly show your work. **[5]**

50MHz = 20ns

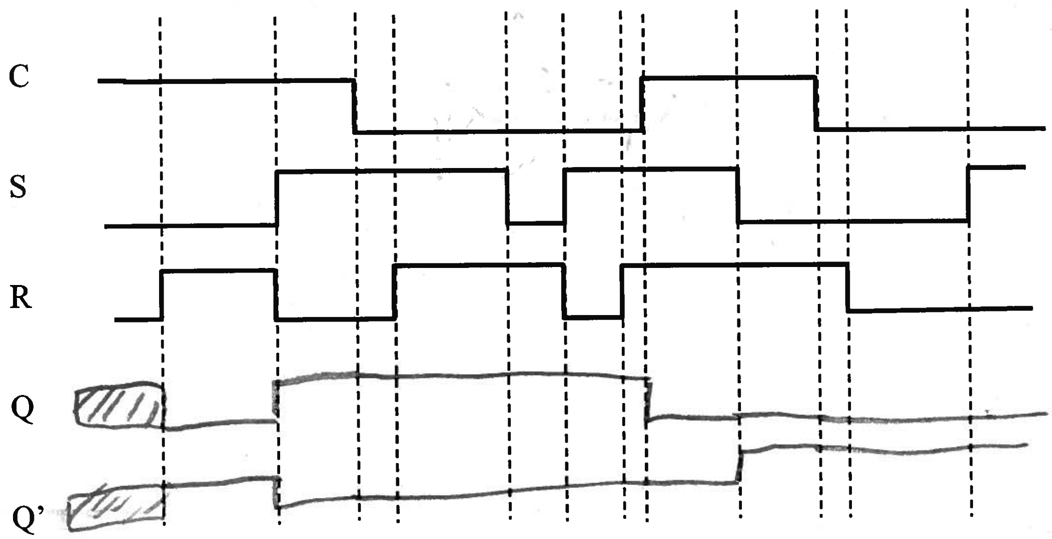
0

longest delay from ↑ of Clock is 20 ns. So 0ns setup time

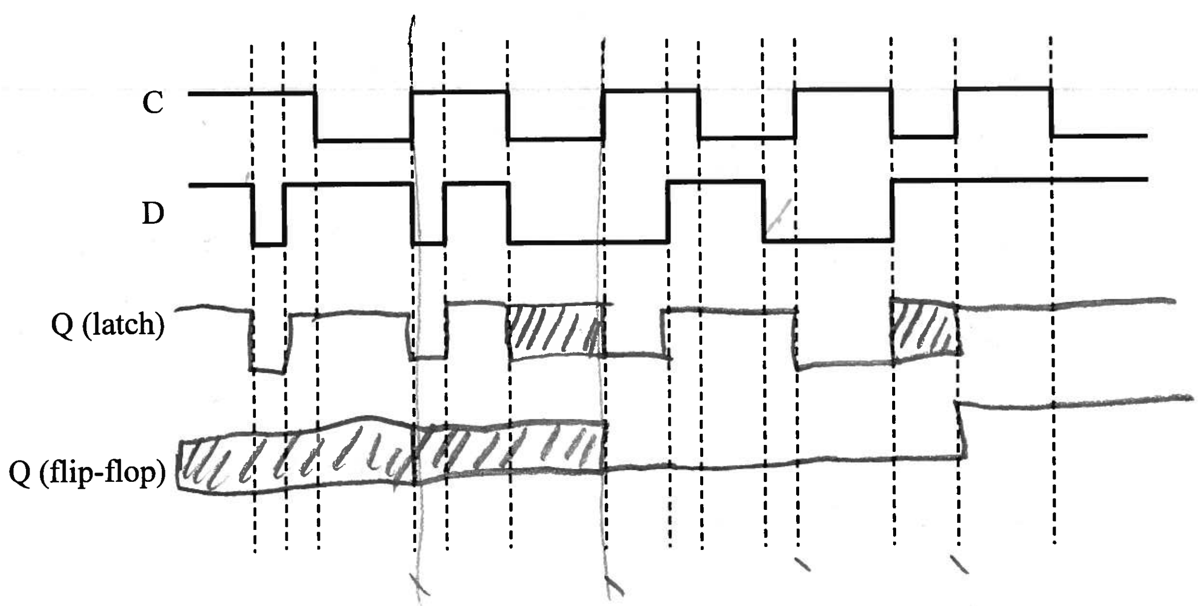
4. Complete the following timing diagrams. If the value is unknown (or oscillating) at some point, clearly indicate that with hashes (as shown). **[12 points]**



a) Complete the timing diagram below for an SR latch with enable. **[6]**

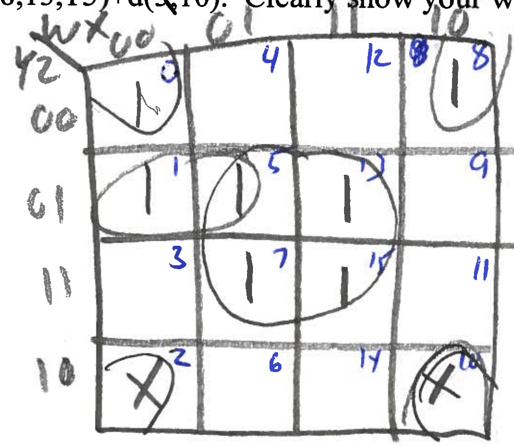


b) Complete the timing diagram below for both a D latch and a D flip-flop. **[6]**



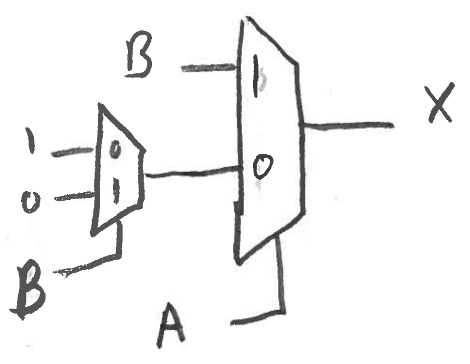
2

5. Find the minimum sum-of-products for the following function:
$F=\sum_{WXYZ}(0,1,5,7,8,13,15)+d(\cancel{5},10)$. Clearly show your work via a Kmap. **[8 points]**



$\bar{X}\bar{Z} + \bar{W}\bar{Y}Z + XZ$

6. Using only two 2-to-1 MUXes, implement an XNOR gate with inputs A, B and an output X. You may freely use 0 and 1 as inputs as needed. **[5 points]**



A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

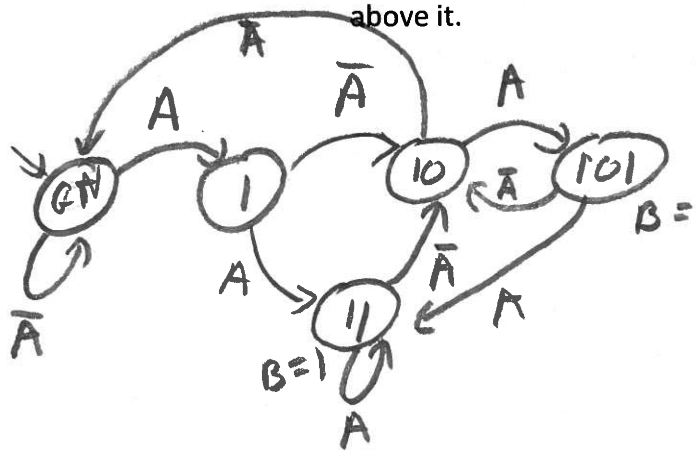
if A=1, output B
if A=0 output $\bar{B}$

7. Design a state transition diagram for each of the following. **[12 points]**

a) The machine has one input A and one output, B. The output is to go high if the most recent values of A has been either "101" or "11", otherwise the output is to be low. **[6]**

```
A:1011001010111
B:0011000010111
```

← This is the output after the machine sees the A value immediately above it.

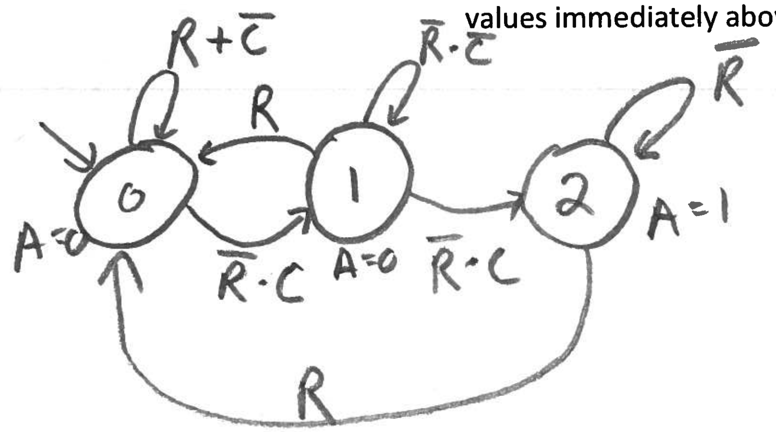


B=0 if not shown

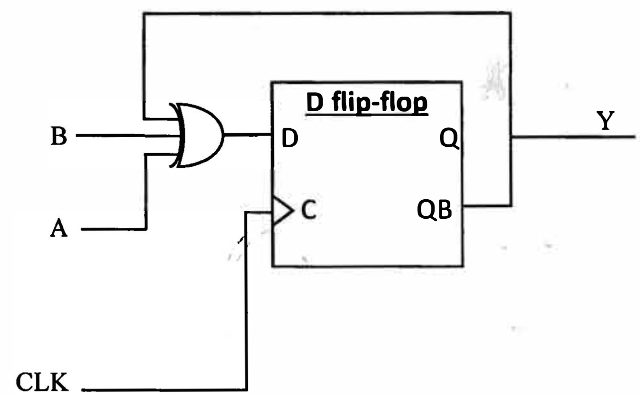
b) The machine has two inputs C and R and one output A. A should go high only if C has been high for at least two cycles since R last was high. Be sure to look at the example carefully. **[6]**

```
R:1000000010000111000000
C:0110010001001110111111
A:0011111100001000011111
```

← This is the output after the machine sees the C and R values immediately above it.



8. Write a Verilog module, Bob, which implements the following circuit. The code must be correct, clear, and reasonably concise to get full points. **[9 points]**

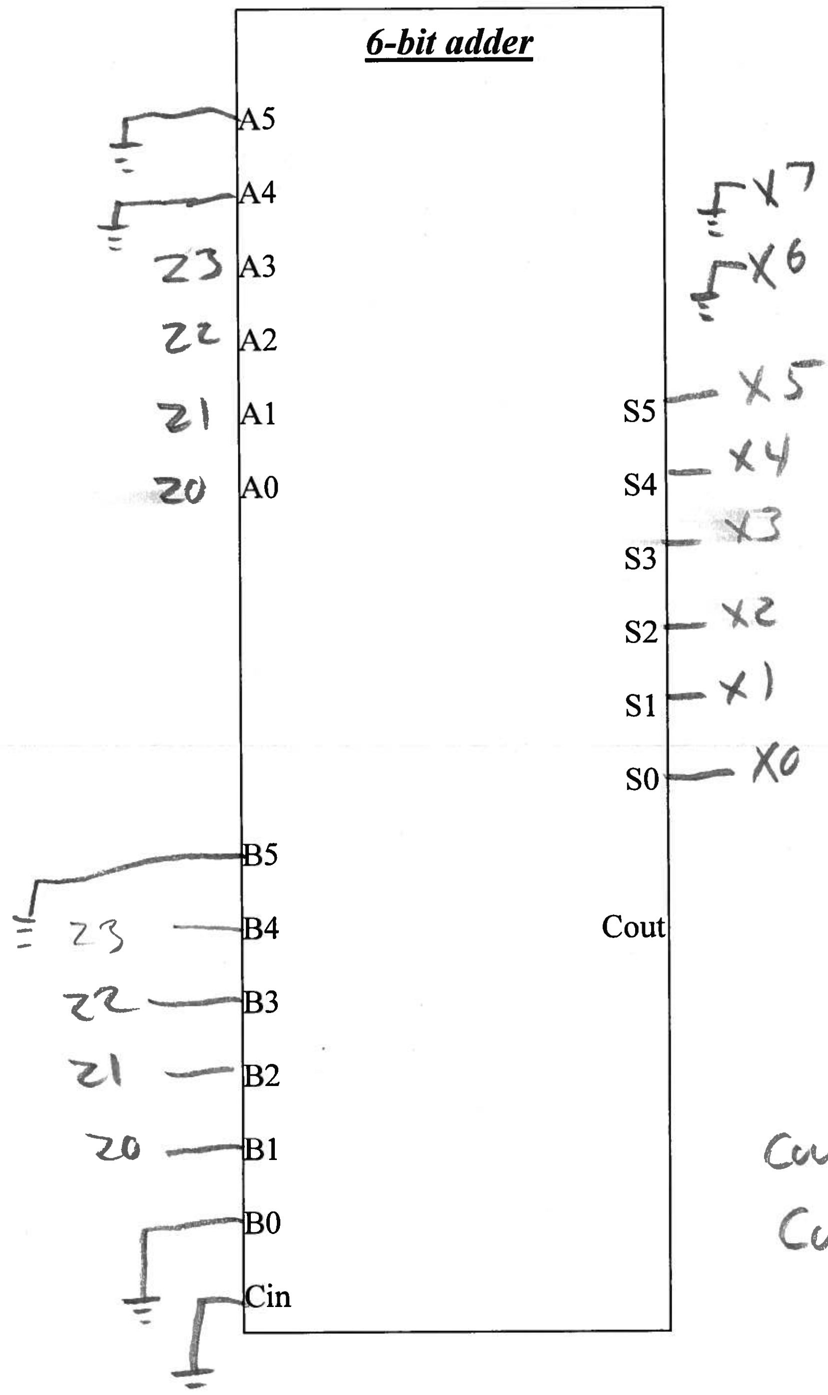



```
module fsm1(
     input   CLK, A, B,
     output       Y);

     reg Q;
     always@(posedge CLK)
          Q = ~Q^A^B;

     assign Y = ~Q;

endmodule
```

There are a number of ways to have done this, but the above is probably the easiest.

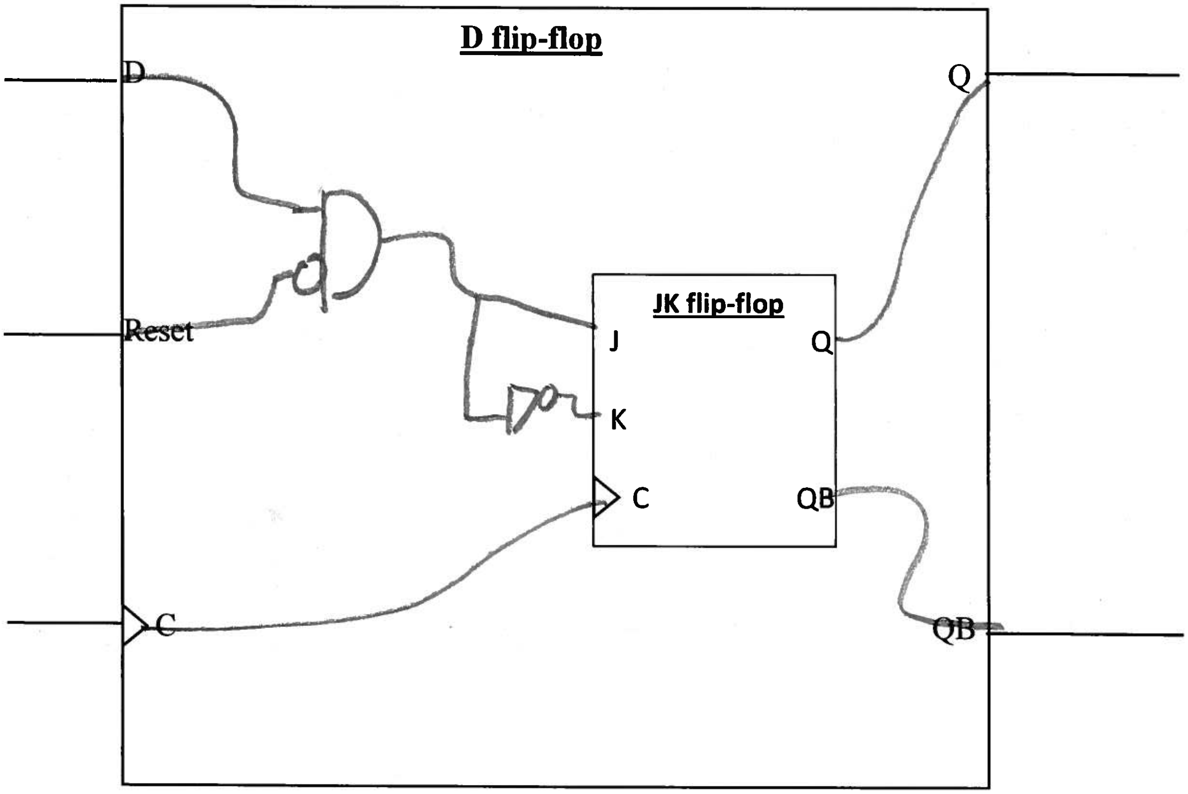
9. Design a circuit which has as an input Z[3:0] and output X[7:0] where both are treated as unsigned numbers. X should be equal to 3 times Z's value. You may only use:
   - One 6-bit adder (with carry in and carry out), drawn below.
   - Up to three NOT gates (you may use bubbles to represent these)
   - Power and ground.

   As always, you may not need all of those devices. **[9 points]**



Could use Cout for X6 or X7

10. Build a D flip-flop with reset using only a JK flip-flop and standard gates. **[10 points]**



Recall:

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

D	R	Q	S	K
0	0	0	0	1
0	1	0	0	1
1	0	1	1	0
1	1	0	0	1

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