Quiz 1 – Spring 2023 – EECS 270

Name: Key uname: _____

This quiz is graded out of 100 points. Please remember you can drop your lowest quiz score. You will have 20 minutes for the quiz. It is closed book and closed notes. Show your work.

1. Convert the following into canonical sum-of-products representation: X= A*B+!A*C. **[25]**

X = $ABC + AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$

2. Fill-in-the-blank **[25 points]**

-8 ≤1

a. The 4-bit 2's complement number representation of -5 is 1011.

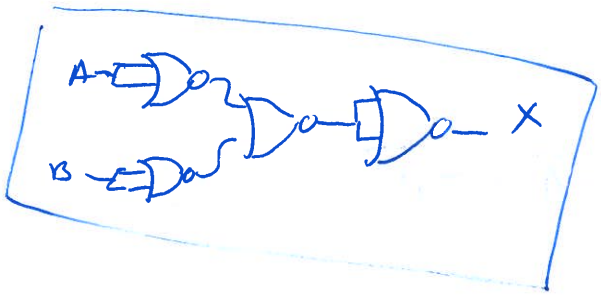
b. The 6-bit signed-magnitude representation of -5 is 100101.

c. The range of representation for a 5-bit 2's complement number is from -16 to 15.

d. According to the Commutative theorem of Boolean algebra, A*B = B*A.

e. (A+B)*(A+C) = A + BC according to the distributive theorem.

3. Implement a 2-input NAND gate using only 2-input NOR gates. For full credit, use 4 or fewer NOR gates. **[25]**



4. Using only the devices listed below, design a circuit which takes two 3-bit unsigned numbers (C[2:0], D[2:0]) as inputs and outputs a 4-bit unsigned number (X[3:0]). The result should be the bitwise AND of C and D (with X[3]=0) if C=D, otherwise it should be the sum of C and D. You have the following components available
    - A 3-bit 2-to-1 MUX
    - 4-to-2 priority encoder
    - A 3-bit unsigned comparator (has equal and greater-than outputs)
    - A 3-bit adder (inputs are A[2:0], B[2:0], and Cin. The outputs are S[2:0] and Cout).
    - NOT gates
    - 2-input AND, OR, XOR and XNOR gates

    You must clearly label any device you use (other than those that are clear by shape) and your design should be clear enough that someone else could understand how everything was to be connected. *Your grade will be based in part upon the efficiency and clarity of your design.* **[25]**