Quiz 2 – Spring 2023 – EECS 270

Name: _____ uname: _____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

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1. Fill-in-the-blank **[20 points, -5 for each wrong or blank answer]**

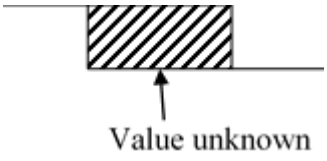
    a. The time *before* the rising edge of the clock when no input should be changing after is called the _____

    b. _____ is -7 as a 5-bit 2's complement number

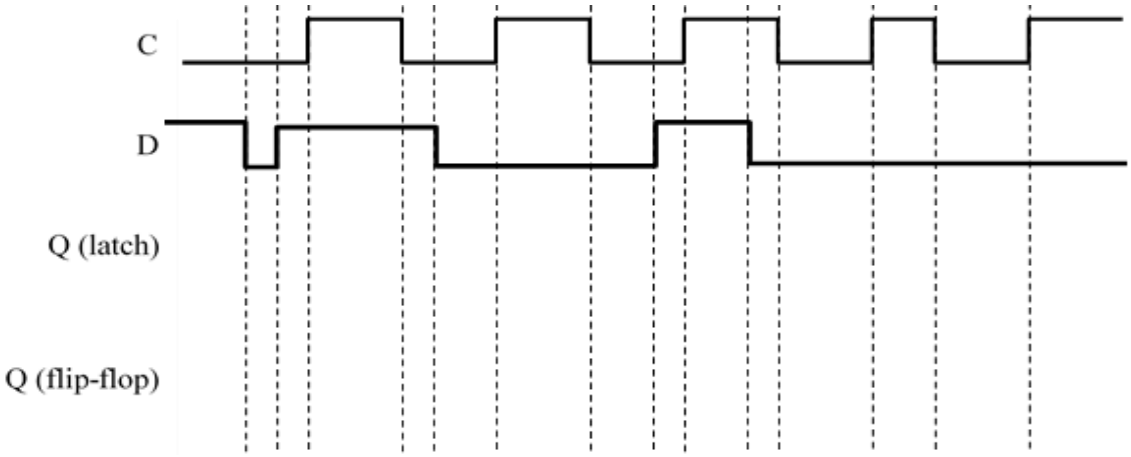
    c. A signal with a frequency of 10MHz has a period of _____ns

    d. !(A+!B+C), when expanded into canonical sum-of-products form, has _____ minterms.

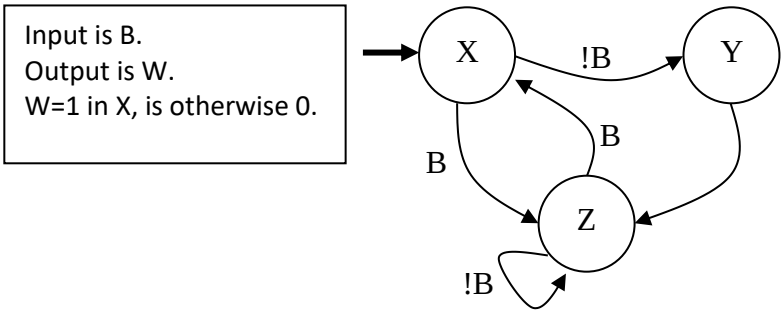
2. Answer the following questions:
    a. Draw gates which implement a D-latch. **[15]**



b. Complete the timing diagram below for both a D latch and a D flip-flop. If the value is unknown at some point, clearly indicate that with hashes (as shown). **[20 points]**



3. Design a state machine which implements the following state transition diagram. Assign state bits **S[1:0] as 00 for state X, 10 for state Y, and 11 for state Z**. You are to assume that you will never reach the state S[1:0]=10, so you don't care what happens in that case. You must show your work to get any credit! *You only need to compute the next state and output logic, you don't need to draw the gates or flip-flops!* Place your answer where shown, all answers must be in *sum-of-products* form. **[45 points]**



(Be sure all are in sum-of-products form (canonical or otherwise)!)

NS1= _____

NS0= _____

W= _____