

## Quiz 2 – Spring 2023 – EECS 270

Name: \_\_\_\_\_ uname: \_\_\_\_\_

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

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### 1. Fill-in-the-blank [20 points, -5 for each wrong or blank answer]

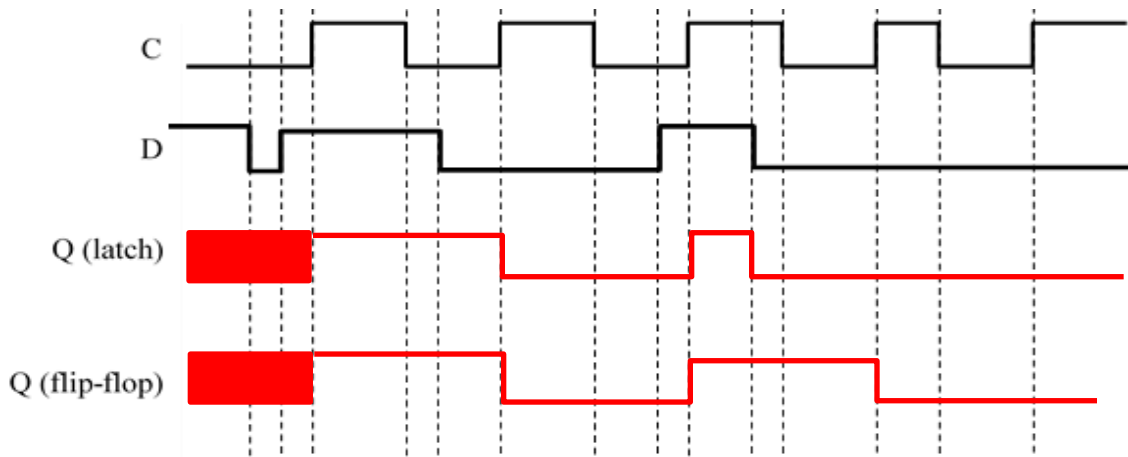
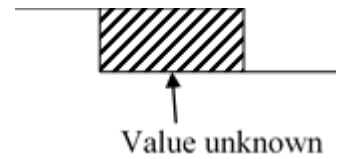
- a. The time *before* the rising edge of the clock when no input should be changing after is called the setup time
- b. 11001 is -7 as a 5-bit 2's complement number
- c. A signal with a frequency of 10MHz has a period of 100 ns
- d.  $\overline{A+B+C}$ , when expanded into canonical sum-of-products form, has 1 minterms.

$$\overline{A+B+C} = \overline{A} * \overline{B} * \overline{C}$$

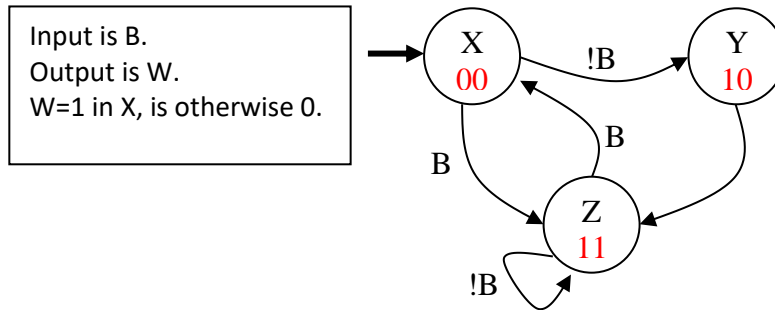
2. Answer the following questions:
- Draw gates which implement a D-latch. [15]

See text.

- Complete the timing diagram below for both a D latch and a D flip-flop. If the value is unknown at some point, clearly indicate that with hashes (as shown). [20 points]



3. Design a state machine which implements the following state transition diagram. Assign state bits **S[1:0]** as **00 for state X, 10 for state Y, and 11 for state Z**. You are to assume that you will never reach the state S[1:0]=01, so you don't care what happens in that case. You must show your work to get any credit! You only need to compute the next state and output logic, you don't need to draw the gates or flip-flops! Place your answer where shown, all answers must be in sum-of-products form. [45 points]



| S1 | S0 | B | NS1 | NS0 |
|----|----|---|-----|-----|
| 0  | 0  | 0 | 1   | 0   |
| 0  | 0  | 1 | 1   | 1   |
| 0  | 1  | 0 | DC  | DC  |
| 0  | 1  | 1 | DC  | DC  |
| 1  | 0  | 0 | 1   | 1   |
| 1  | 0  | 1 | 1   | 1   |
| 1  | 1  | 0 | 1   | 1   |
| 1  | 1  | 1 | 0   | 0   |

$$NS1 = !S1 + !S0 + !B$$

$$NS0 = S1 * !B + !S0 * B$$

(Be sure all are in sum-of-products form (canonical or otherwise)!)

$$NS1 = !S1 + !S0 + !B \underline{\hspace{10em}}$$

$$NS0 = S1 * !B + !S0 * B \underline{\hspace{10em}}$$

$$W = !S1 \underline{\hspace{10em}}$$