Quiz 4 – Spring 2011 – EECS 270

Name: KEY uname: _____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

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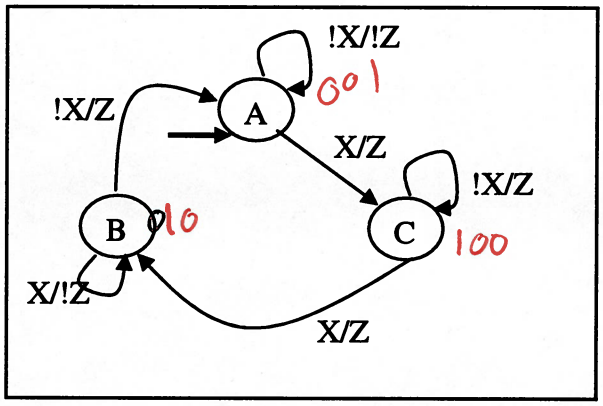
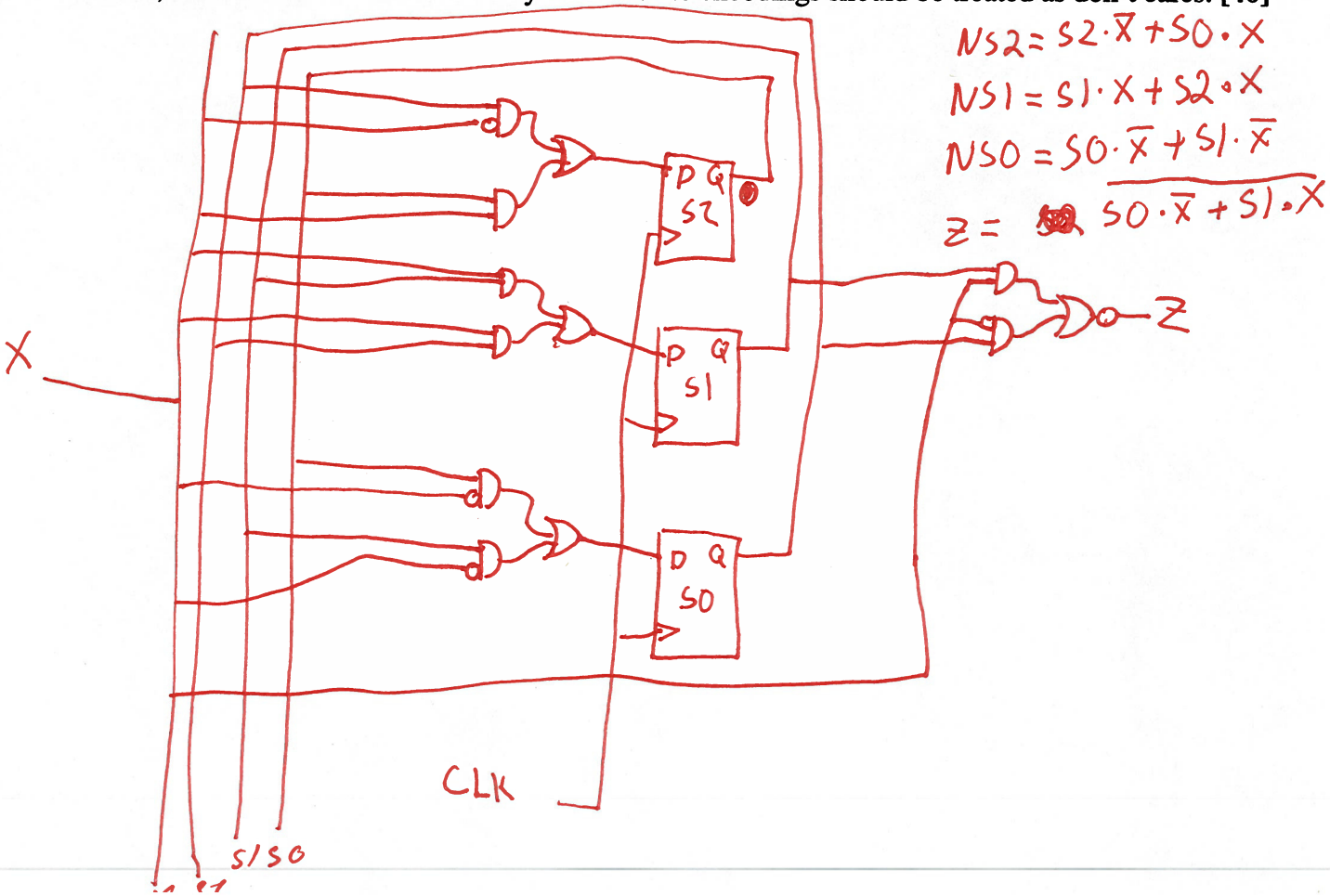
1. Consider the following state-transition diagram:



Using only AND, OR, and NOT gates (including freely using bubbles) as well as D flip-flops, *draw* the state machine for the above state-transition diagram. You are to use an encoding of A=001, B=010, and C=100 for the states. Any unused state encodings should be treated as don't cares. **[40]**

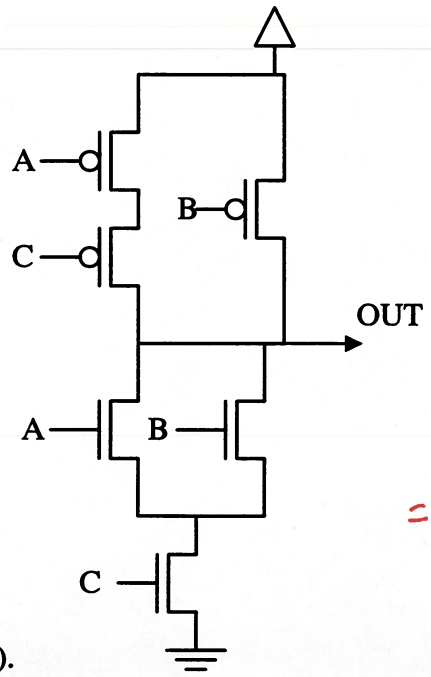


=1 if B=0 or A+Bbar=0

2. Transistor problem. **[30]**

A	B	C	OUT		
0	0	0	1		1
0	0	1	1		1
0	1	0	1		1
0	1	1		0	0
1	0	0	1		1
1	0	1	1	0	smoke
1	1	0			Hiz
1	1	1		0	0

Fill in the above truth table with either "1", "0", "Hi-Z" or "Smoke" (the last if OUT is connected to both Vcc and Ground).

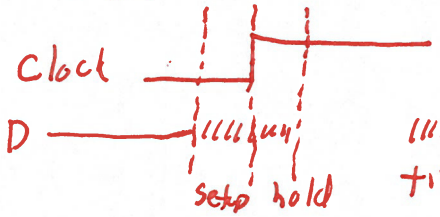


=0 (A+B)·C

3. It is November 2011 and you've got a friend taking EECS 270 who are really confused about set-up and hold times.

a. Clearly explain what set-up time and hold time *are* on a D flip-flop. Include a simple sketch. **[10]**

Hold time ~~is~~ and setup time are the times before + after the rising edge of the clock (respectively) when the D input is not allowed to change.



IIII = d must remain constant during this time

b. Explain how set-up time impacts a circuit design in 35 words or less. **[10]**

~~Setup time~~ Because the data must remain steady for a some time before the clock edge, this ends up increasing the required clock period.

c. Explain how hold time impacts a circuit design in 35 words or less. **[10]**

We must insure that the fast path (min path) through the circuit ~~is~~ isn't faster than the hold time. If it is we must add delay.