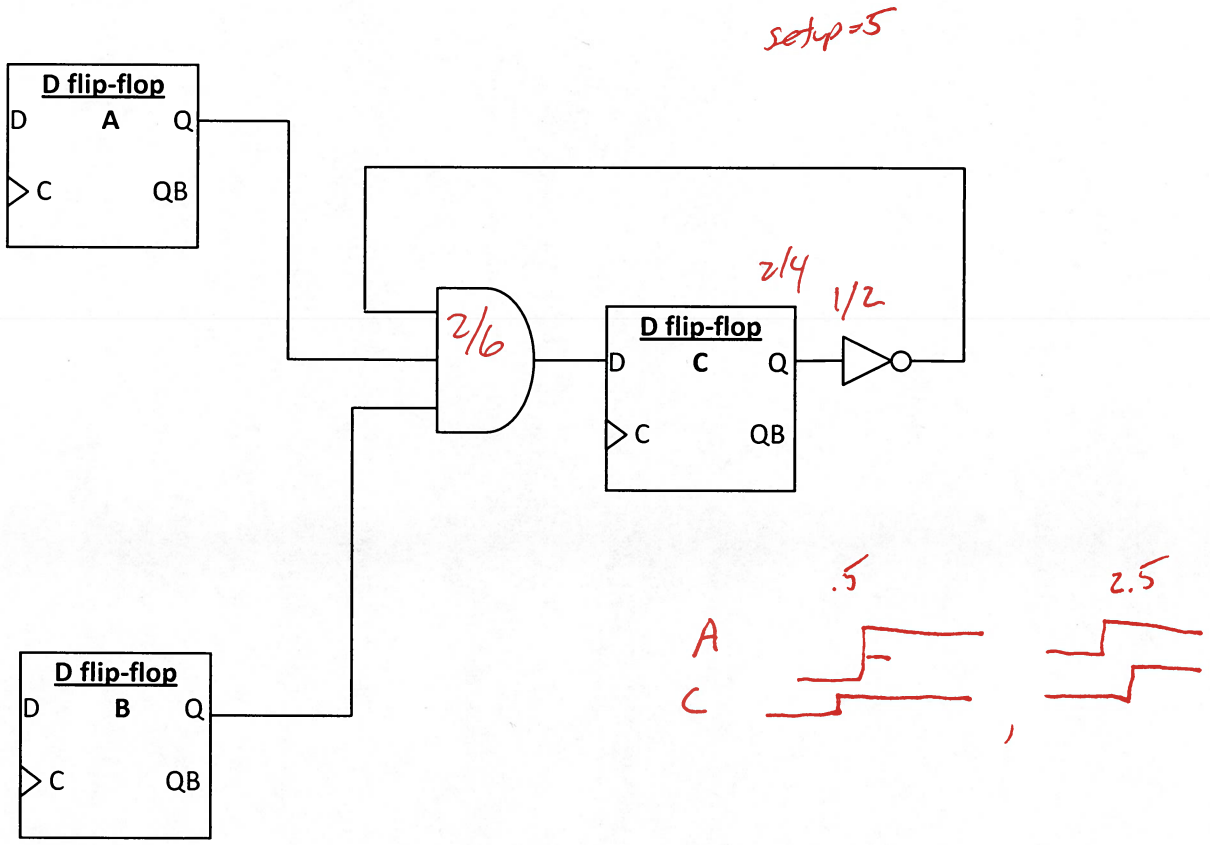
Quiz 5 EECS 270 Spring 2011. Honor code applies.

Name: KEY uname: _____



1) Consider flip-flops A, B and C, each nominally clocked off of the same clock. Assume
   - Each flip-flop has a set-up time of 5ns and a clock-to-Q delay of 2ns to 4ns.
   - The AND gate has a delay of 2 to 6ns.
   - The NOT gate has a delay of 1 to 2 ns.
   - Flip-flops A and B have no clock skew between them.
   - Flip-flop C's rising edge may be as much as 0.5 ns before A and B's rising edge or as much 2.5ns after.

   a) What is the fastest clock period you could safely clock this system at? **[10]**

   CtoQ 4, CLD 8 setup 5 = 17ns

   b) What is the (non-negative) range of values for the hold time that would be sufficient? **[10]**

   0 to 1.5 ns

   c) Redo part a) assuming the NOT gate always had a delay of 0ns **[10]**

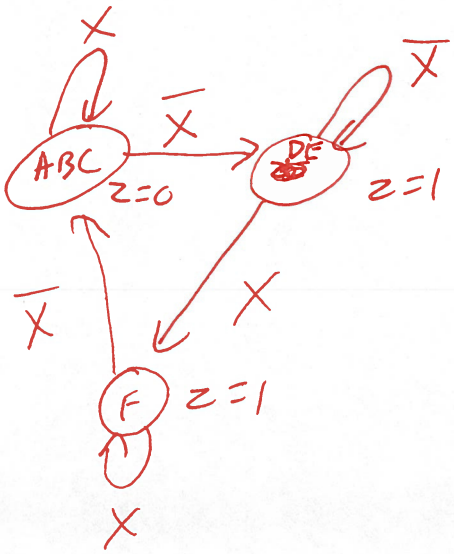
   4 + 6 + 5 + .5 = 15.5ns

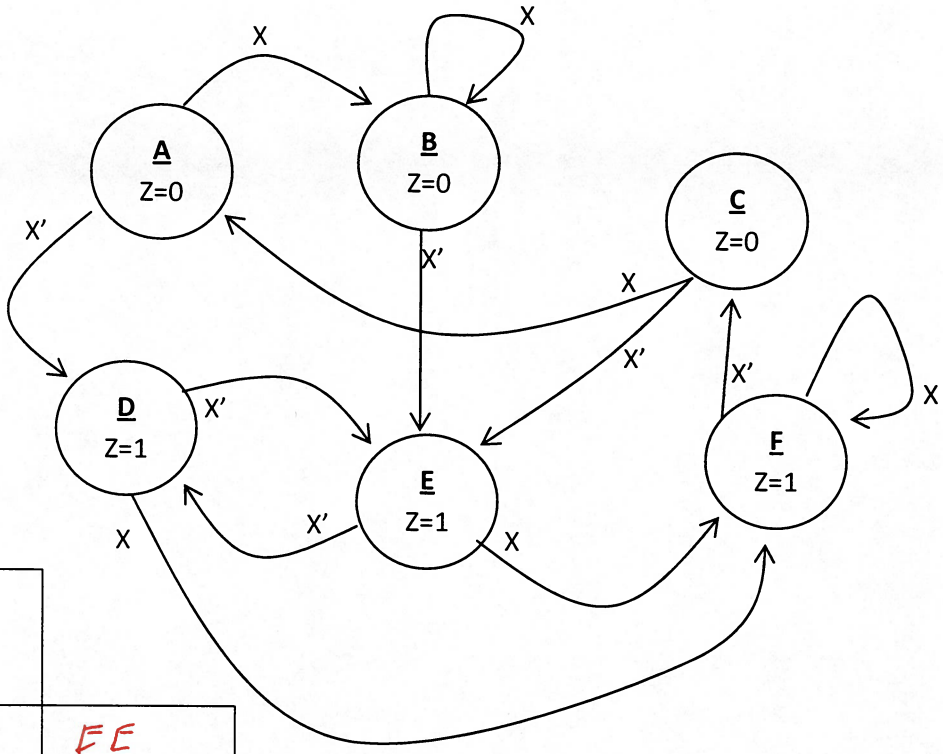
   d) Redo part b) assuming the NOT gate always had a delay of 0ns. **[10]**

   0 to 1.5ns

Quiz 5 EECS 270 Spring 2011. Honor code applies.

2) Reduce the number of states in the state transition diagram as much as possible using the partitioning method. Show your work and draw the reduced state diagram.





A	X				
B	X	E, D B, B			
C	X	E, D A, B	FE A B		
D	~~E, C~~ ~~F, F~~	X	X	X	
E	~~D, C~~ ~~F, F~~	X	X	X	D, F F F
	F	A	B	C	D