Quiz 1 – Spring 2007 – EECS 270

Name: Key uname: _____

This quiz is graded out of 100 points. Please remember you can drop your lowest quiz score. You will have 20 minutes for the quiz. It is closed book and closed notes. Show your work and ***circle your answer!***

1. Convert the following to canonical sum-of-products using any method. F=(A+A'B')*C' **[25]**

$A\bar{C} + \bar{A}\bar{B}\bar{C} \leftrightarrow AB\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$

2. What is the range of representation for the following schemes? **[20 points, -3 per wrong or blank answer, min 0]**

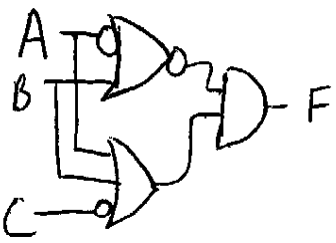
   a. 5-bit 2's complement -16 to 15

   b. 3-bit 2's complement -4 to 3

   c. 5-bit unsigned 0 to 31

   d. 5-bit signed-magnitude -15 to ±15

3. Draw the logic gates which correspond to the following logical statement F=(A'+B)'*(A+C'+B) **[15]**

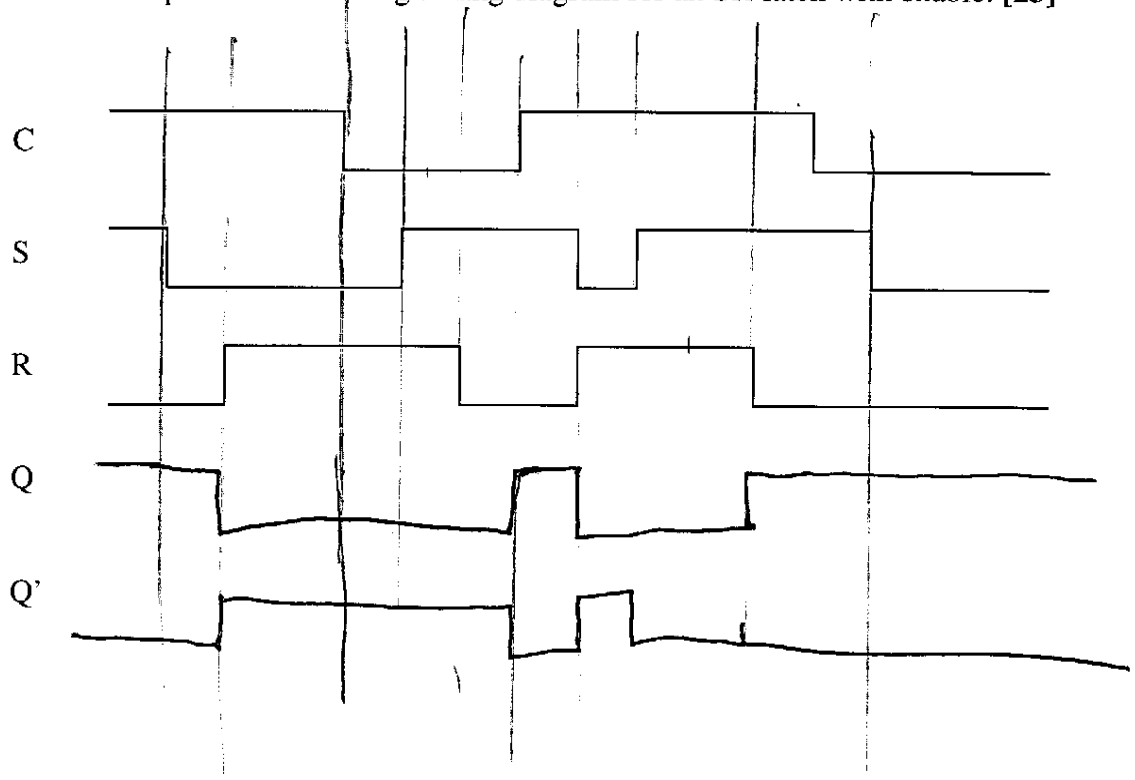


4. Use perfect induction to prove (some version of) DeMorgan's law **[15]**

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

A	B	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

5. Complete the following timing diagram for an SR-latch with enable. **[25]**



Quiz 2 – Spring 2007 – EECS 270

Name: Key uname: _____

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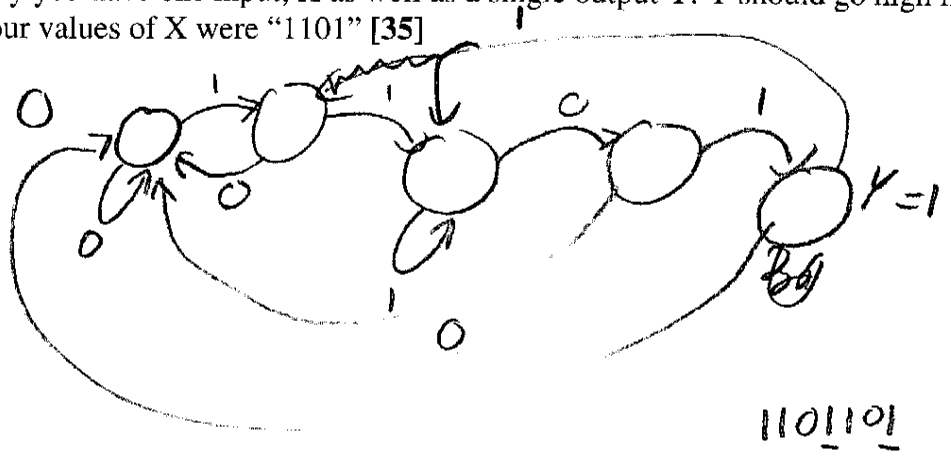
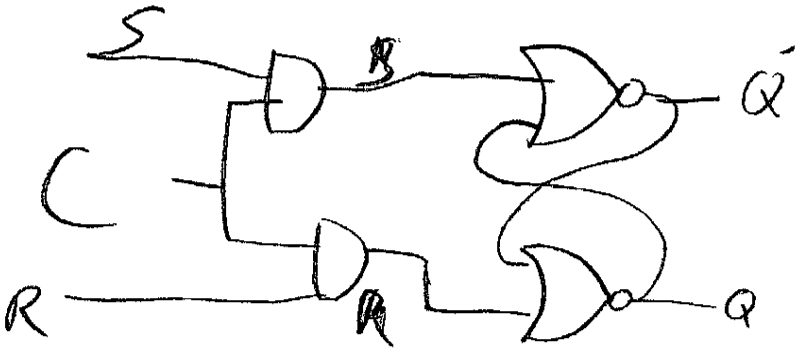
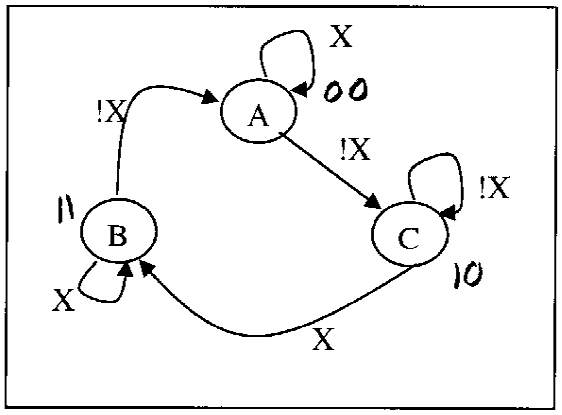
1. Say you have one input, X as well as a single output Y. Y should go high iff the last four values of X were "1101" **[35]**



2. Draw an SR-latch with enable using only gates (AND, OR, NOT) and inversion bubbles. Correctly label all the inputs and outputs. **[20]**



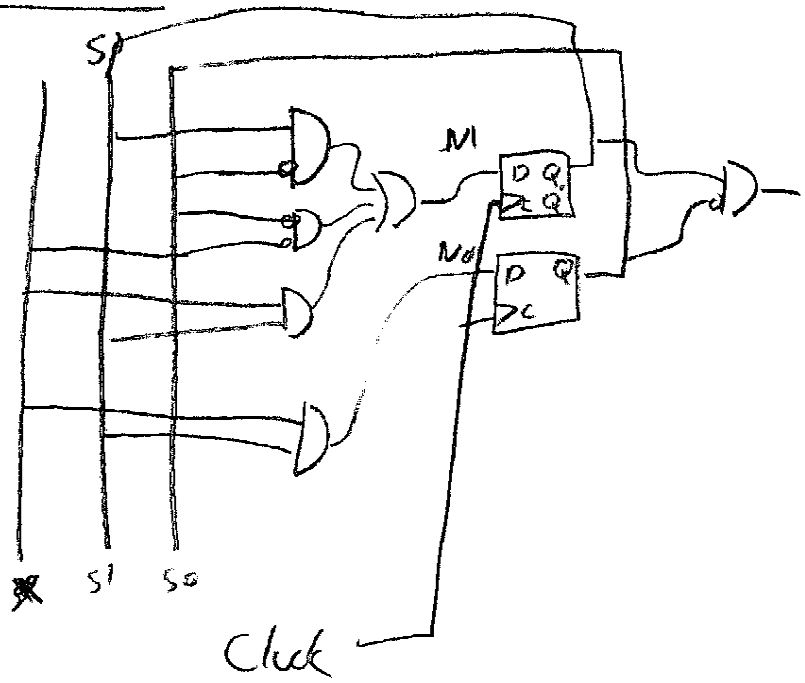
3. Consider the following state-transition diagram:



There is one output, Z, which is 1 when in state A and 0 in states B and C.

Using only AND, OR, and NOT gates (including freely using bubbles) as well as D flip-flops, *draw* the state machine for the above state-transition diagram. You are to use an encoding of A=00, B=11, and C=10 for the states. Finally, any unused state encodings should be treated as don't cares. **[45]**

S1	S0	X	N1	N0
0	0	0	1	0
0	0	1	0	0
0	1	0	—	
0	1	1	—	
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1



$N1 = S1\,\overline{S0} + \overline{S0}\,\overline{X} + S1\,X$

$N0 = S1\,X$

$Y = S1\,\overline{S0}$