Quiz 3 – EECS 270, Spring '07

Name: KEY unique name: KEY

Honor code:
I have not given or received aid on this quiz, nor have I observed anyone else doing so:

Sign here:_____

This quiz is graded out of 100 points and is worth about 3% of your class grade. You will have **25** minutes for this quiz. ***Closed everything including calculators!*** To receive partial credit, work must be shown.

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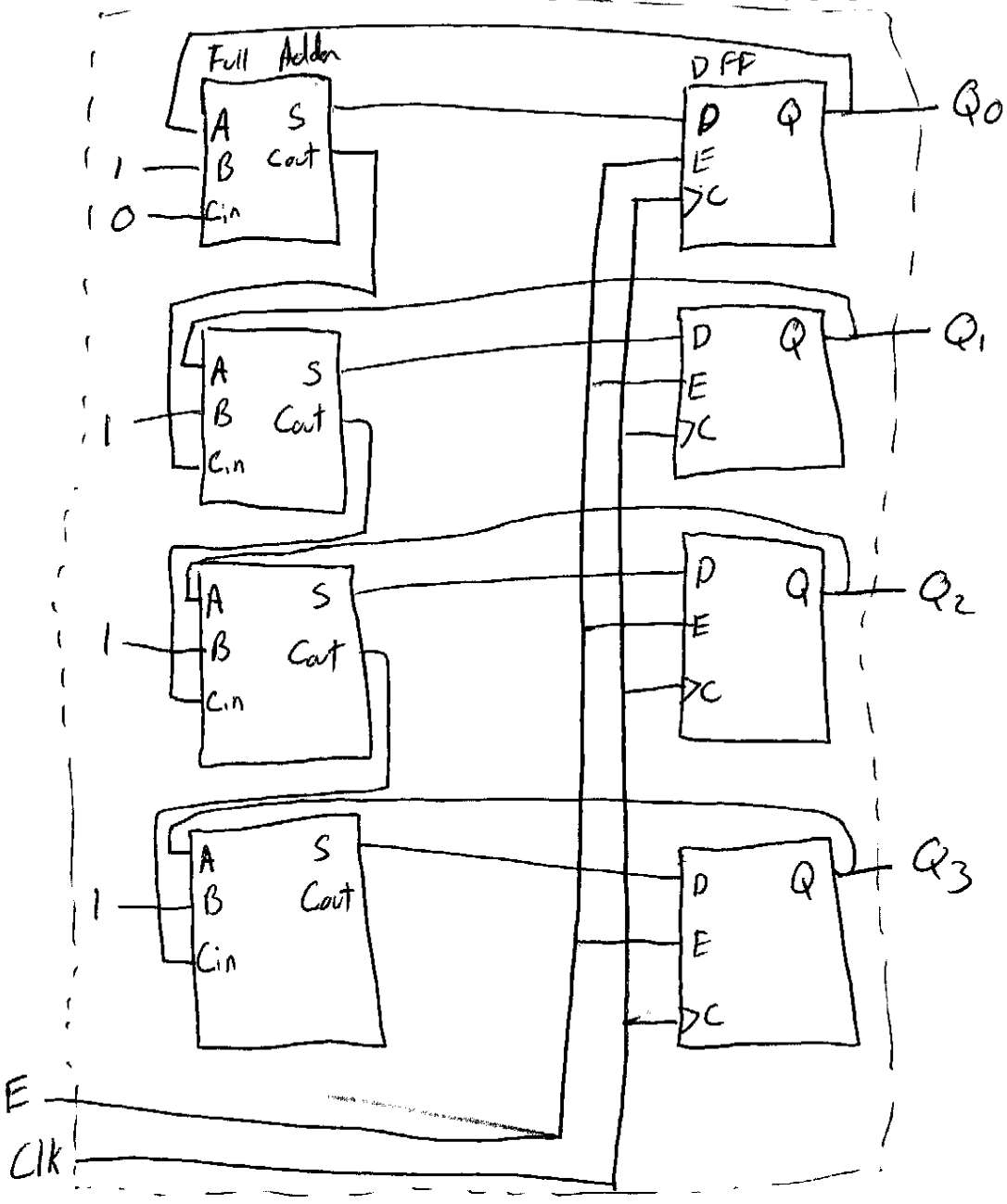
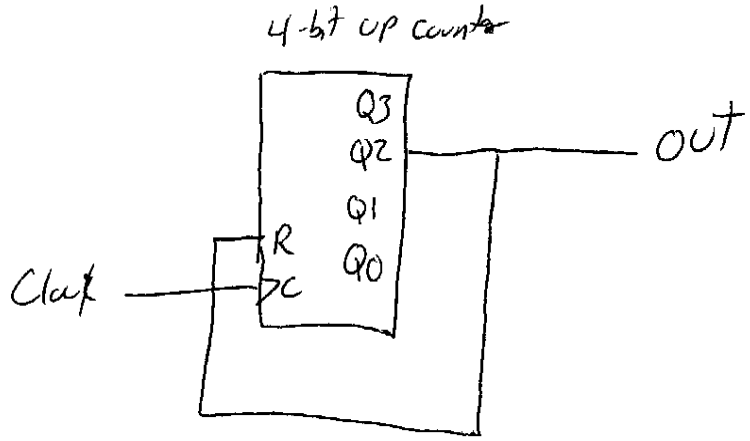
1. Design a 4-bit down counter with enable using only MUXes, encoders, 1-bit full adders, decoders, and D flip flops (with enable). **[50]**

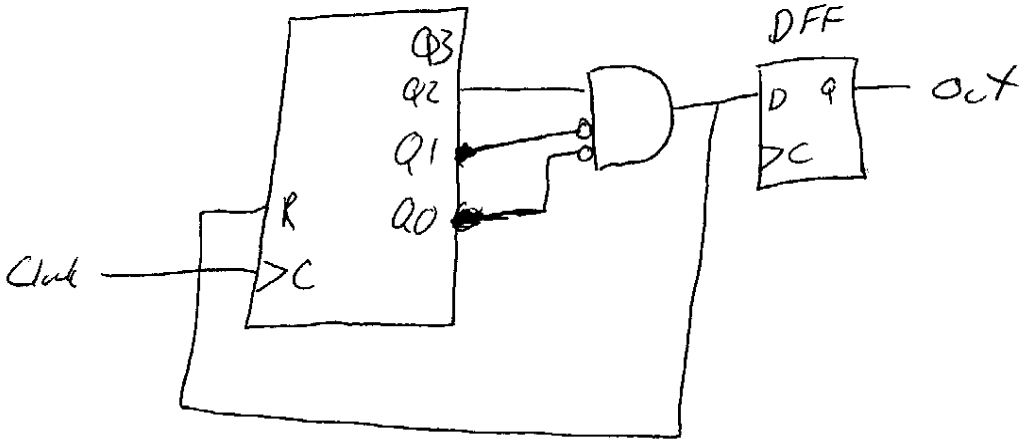


with reset ← added before quiz

2. Using a 4-bit up-counter and standard gates, design a circuit that outputs a "1" every 5th cycle (otherwise the output is zero). This is called a "divide by 5" device as the output frequency will be one-fifth the original clock frequency. **[50]**



More generic



You should understand why the DFF isn't needed in the first design, but might be needed in the second.