# Quiz 2 – Spring 2011 – EECS 270
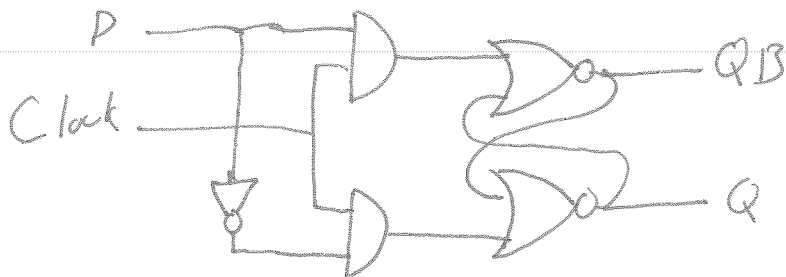
Name: _KEY_____ uname: _K.EY_____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.
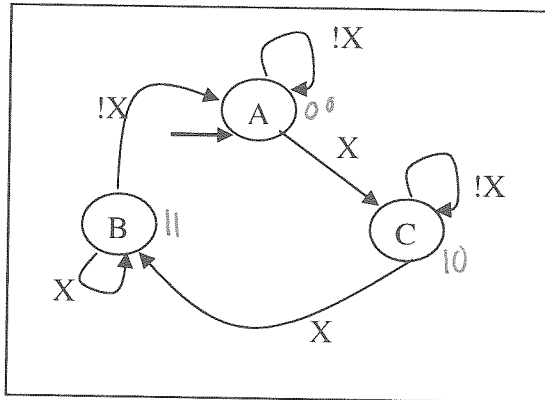
1. Say you have one input, X as well as a single output Y. Provide a state-transition diagram where Y goes high iff the last three values of X were "101" [30]
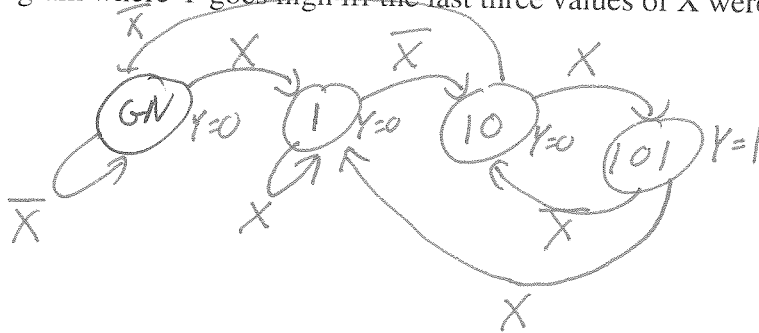
2. Draw a D-latch using only ANDs, ORs, and NOTs (you may represent a NOT as a bubble, but you must do so clearly). You must clearly label the inputs and outputs as in the standard way (D, Clock, Q, QB) [25]

S1	S0	X	NS1	NS0
0	0	0	0	0
0	0	1	1	0
0	1	0	D.C	D.C
0	1	1	D.C	D.C
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

3. Consider the following state-transition diagram:

$$NS1 = X + S1\,\overline{S0}$$
$$NS0 = S1 \cdot X$$
$$Z = \overline{S1}$$

There is one output, Z, which is 1 when in state A and 0 in states B and C.

Using only AND, OR, and NOT gates (including freely using bubbles) as well as D flip-flops, _draw_ the state machine for the above state-transition diagram. You are to use an encoding of A=00, B=11, and C=10 for the states. Finally, any unused state encodings should be treated as don't cares. [45]