Quiz 1 – Spring 2013 – EECS 270

Name: KEY uname: _____

This quiz is graded out of 100 points. Please remember you can drop your lowest quiz score. You will have 15 minutes for the quiz. It is closed book and closed notes. Show your work and ***circle your answer!*** The last problem is quite hard and worth fewer points…

1. Convert the following to canonical ***sum-of-products*** using any method. **[30]**

   F=(A+B+C)*!(A+D) **[30 points]**

$(A+B+C)\cdot\bar{A}\cdot\bar{D}$

$\bar{A}A\bar{D} + \bar{A}B\bar{D} + \bar{A}C\bar{D}$

$\bar{A}BC\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + \bar{A}\bar{B}C\bar{D}$

same

$\bar{A}BC\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D}$

00101
11010
11011

2. Fill-in-the-blank **[25 points, -5 for each wrong or blank answer, minimum 0]**

   a. The 5-bit 2's complement number representation of -5 is 11011.

   b. 10001, when treated as a 5-bit signed-magnitude number, has a decimal representation of -1.

   c. NOR gates and NAND gates are each logically complete.

   d. The range of representation for a 6-bit unsigned number is from 0 to 63.

3. Using only the devices listed below, design a circuit which takes two *3-bit signed numbers* (X[2:0] and Y[2:0]) and outputs the smaller of the two, named OUT[2:0]. (If the inputs have the same value, you can output either).

   In your design you may use the following devices (as well as freely using "0" and "1" as a inputs as desired)

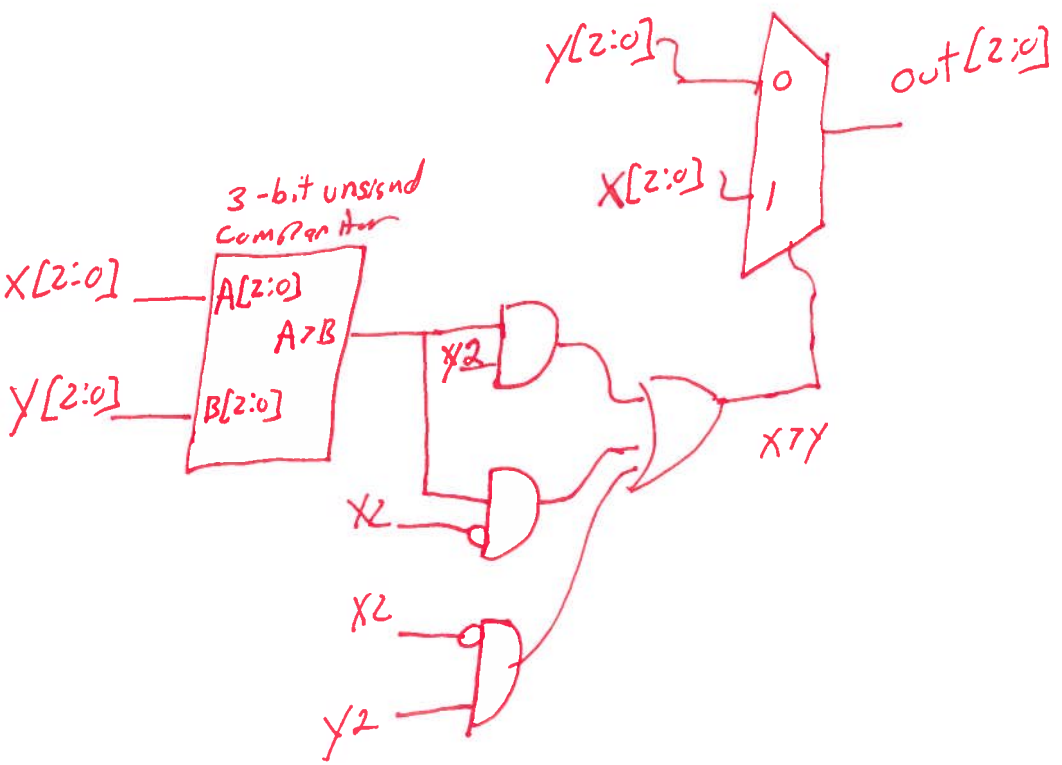
   - AND, OR, and XOR gates (any number of inputs)
   - Inverters
   - 1-bit 2 to 1 MUX
   - 3-bit *unsigned* comparator (has an "equal" and "greater than" output)
   - 3-bit 2 to 1 MUX
   - 8 to 3 priority encoder

   You must clearly label any device you use (other than gates and inverters) and your design should be clear enough that someone else could understand how everything was to be connected. Your grade will be based in part upon the efficiency of your design. **[30]**

This is really hard. Say we use the unsigned comparator to see if X>Y. Call that output "C"

X_2 Y_2 C	X>Y?
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	0
1 0 1	0
1 1 0	0
1 1 1	1

$\Rightarrow \bar{X}_2 Y_2 + \bar{X}_2 C + Y_2 C$



4. Design a device that takes in a 4-bit 2's complement number and outputs a 5-bit 2's complement number that is twice the value. You may use standard gates, but are to use as few gates as possible. **[15]**

Trick here is to note that multiplying by 2 ~~is the same~~ in binary is the same as multiplying by 10 in decimal → just adds a zero.

1111 → 11110
(-1) (-2)

0001 → 00010
(1) (2)