Quiz 2 – Spring 2013 – EECS 270

Name: KEY uname: KEY

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! To receive partial credit, work must be shown.

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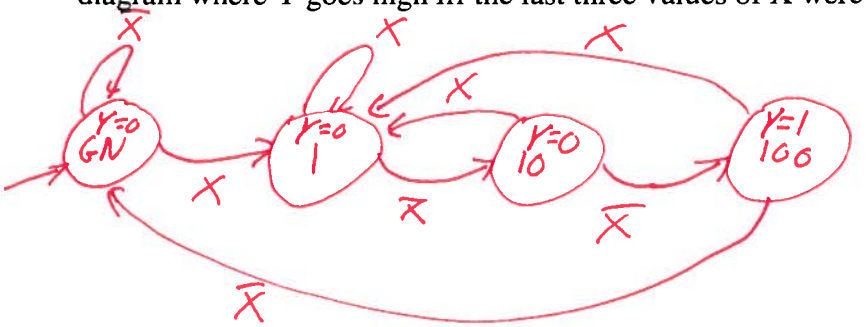
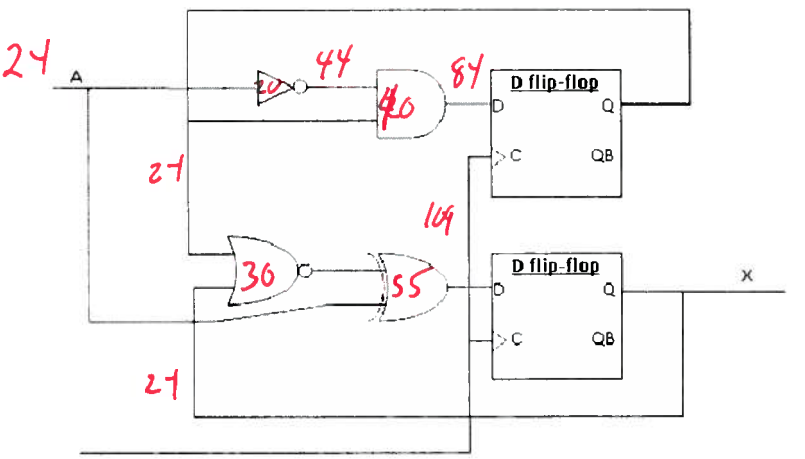
1. Say you have one input, X as well as a single output Y. Provide a state-transition diagram where Y goes high iff the last three values of X were "100". **[30]**



Device	Min	Max
DFF:		
Clock to Q	12ps	24ps
Set-up time	30ps	
Hold time	10ps	
AND/OR	20ps	40ps
NAND/NOR	15ps	30ps
XOR	10ps	55ps
NOT	10ps	20ps

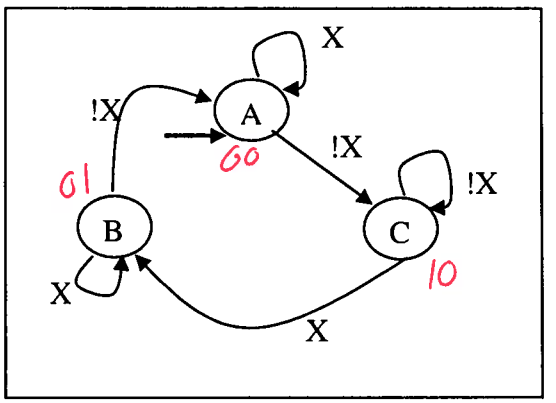


2. Given the circuit and timing information above, what is the lowest clock period you can clock this circuit at? (Hint: the hold time is met so you don't need to add any inverter pairs.) You should assume that the inputs are coming from flip-flops and the outputs are going to flip-flops. *Clearly show your work.* **[30]**

109 + 30 = 139ps

CtoQ + Cpd + set-up

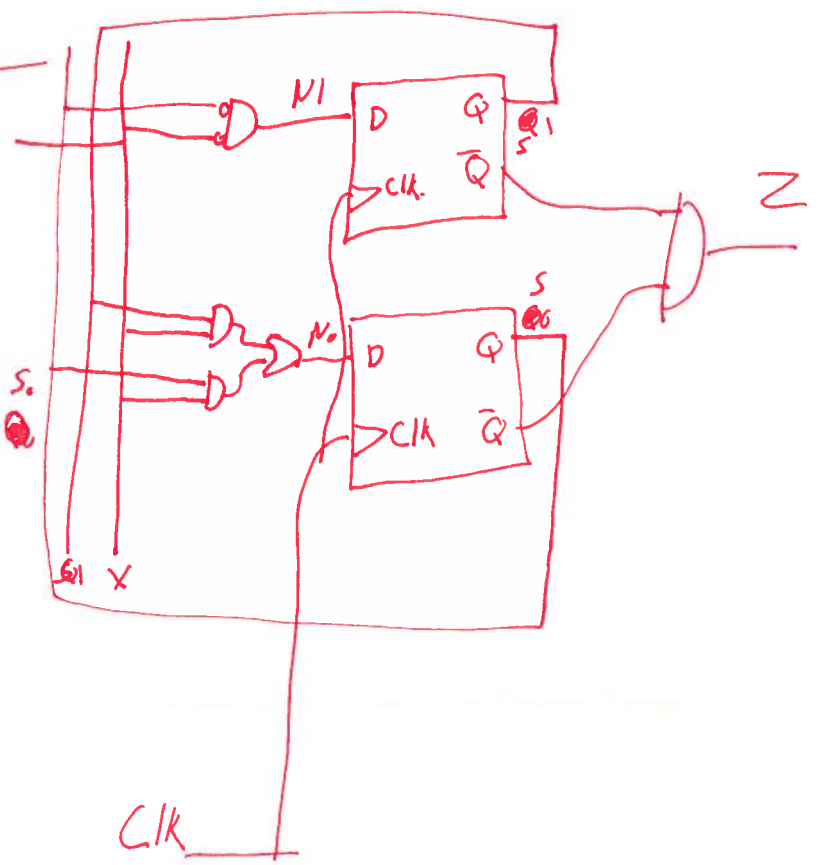
3. Consider the following state-transition diagram:



There is one output, Z, which is 1 when in state A and 0 in states B and C.

Using only AND, OR, and NOT gates (including freely using bubbles) as well as D flip-flops, *draw* the state machine for the above state-transition diagram. You are to use an encoding of A=00, B=01, and C=10 for the states. Finally, any unused state encodings should be treated as don't cares. You need not minimize your logic (though doing so may reduce your work…) **[40]**

S1	S0	X	N1	N0
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	x	x
1	1	1	x	x



$N1 = \overline{S0} \cdot \overline{X}$

$N0 = S0 \cdot X + S1 \cdot X$