Quiz 2 – Spring 2014 – EECS 270

Name: _____ uname: _____

This quiz is graded out of 100 points and is worth about 4% of your class grade. You will have 20 minutes for this quiz. Closed everything including calculators! The last problem could be more work than the points assigned.
To receive partial credit, work must be shown.

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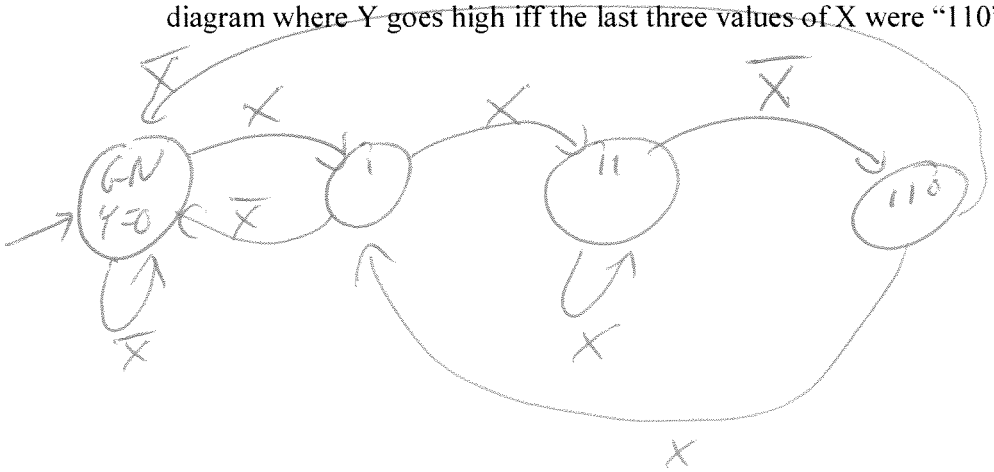
1. Say you have one input, X as well as a single output Y. Provide a state-transition diagram where Y goes high iff the last three values of X were "110". **[30 points]**



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2. Fill-in-the-blank **[20 points, -4 for each wrong or blank answer]**

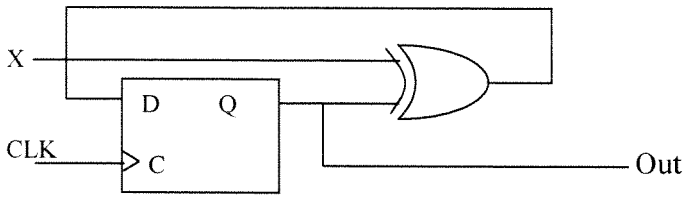
   a. The 5-bit 2's complement number representation of -6 is 11010.

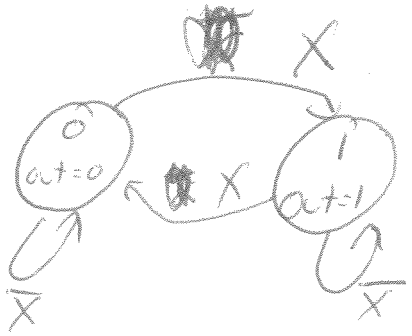
   b. The range of representation for a 6-bit *two's complement* number is from 31 to -32.

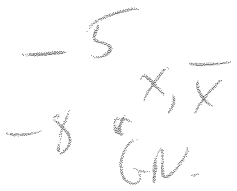
   c. (X+Y)*(X+Z) = X+Y·Z according to the distributive theorem.

   d. The time before the rising edge of the clock when no input should be changing is called the setup

3. Draw a state transition diagram for the following circuit. **[35 points]**







4. Design a 1-bit 4-to-1 MUX using only inverters and tri-state devices. You will be graded in part for having an efficient design. As always, feel free to build a device out of these components and then use that device as needed. **[15 points]**