

Individual Homework 2 -- EECS 270, Fall '09

Due Monday, Sept 28 @2:00pm.

Name: _____ unique name: _____

You are to turn in this sheet as a cover page for your assignment. The rest of the assignment should be stapled to this page. See the website for details about where to turn in your assignment. This is an individual assignment; all of the work should be your own. Assignments that are unstapled, lack a cover sheet, or are difficult to read will lose at least 50% of the possible points and we may not grade them at all.

This assignment is worth about 1% of your grade in the class and is graded out of 30 points. Remember you may drop two assignments (individual or group).

'+'=OR, '*'=AND, '!'=NOT and '^' is XOR.

- Convert the following numbers to 8-bit 2's complement numbers. If the number can't be represented as an 8-bit 2's complement number, write "no such representation". **[2]**
 - 4
 - 4
 - 9
 - 61
 - 127
 - 128
 - 128
 - 0
 - 3
- Convert from the given representations to decimal. **[2]**
 - 10010001, 2's complement
 - 10010001, signed-magnitude
 - 10010001, unsigned
 - 01001, 2's complement
 - 01001, signed-magnitude
 - 11, 2's complement
 - 111, 2's complement
 - 111111, 2's complement
- Add the following numbers as 2's complement values. You are to a) convert each number b) perform the addition showing the sum and carry bits and c) convert 6-bit 2's complement number back into decimal. Notice that part c) could result in getting the wrong answer due to overflow. That "wrong" answer is what we want. **[3]**
 - $-1 + 1$
 - $-4 + -4$
 - $-16 + -16$
 - $16 + 16$
 - $31 + -12$
 - $-25 + -9$
- Using the rules of logic convert the following into sum-of-products form. Show each step as in example 2.13 on page 52. **[4]**
 - $(b*(da)'+c)'$
 - $(a\oplus b)'*(b*c)'$

5. Using only AND, OR, and NOT gates and inversion bubbles draw the gates needed to implement a 4 to 2 priority encoder with an “output enable” output that goes high unless all inputs are zero. Clearly label all wires. **[3]**
6. Using the Sigma notation used in class, describe the sum and carry bit of a full adder. Show your work including the truth table(s). **[3]**
7. You are to design a circuit which takes two 3-bit unsigned numbers, A and B. Its output is a 4-bit unsigned number whose value is the $\min(A,B)+3$. That is, the smaller of A and B is incremented by 3 and sent to the output. You may only use the devices listed below. Each device (other than gates) should be clearly labeled and it should be clear exactly which inputs and outputs of the device are which and where they are going. (see page 82 for a fairly good example of labeling). **[6]**
- Standard 2-input gates (AND, OR, XOR, etc.) as well as NOT gates and inversion bubbles.
 - 3-bit adders (inputs and outputs are both 3-bits) plus carry-in and carry-out.
 - 8 to 3 encoders
 - 3 to 8 decoders
 - 3-bit unsigned comparator (has an EQUAL and GREATER output)
 - 8 to 4 Multiplexors
8. Say that NOT gates have a delay of 50ps, NAND and NOR gates have a delay of 100ps, AND gates have a delay of 150ps, and XOR gates have a delay of 200ps. **[6]**
- a. What is the worst-case propagation delay for the circuit below?
 - b. For the circuit listed below, draw the outputs over time until all signals are in steady state assuming the following things occur:
 - i. Initially all inputs are 0 and have been for a long time. At time 0 B, C, and all go to 1.
 - ii. Initially all inputs are 1 and have been for a long time. At time 0 B and A go to 0. At 200ps D goes to 0.

Show both the outputs and all intermediate signals.

