

# Individual Homework 3 -- EECS 270, Fall '09

Due Monday, Oct 5<sup>th</sup> @2:00pm.

Name: \_\_\_\_\_ unique name: \_\_\_\_\_

You are to turn in this sheet as a cover page for your assignment. The rest of the assignment should be stapled to this page. See the website for details about where to turn in your assignment. This is an individual assignment; all of the work should be your own. Assignments that are unstapled, lack a cover sheet, or are difficult to read will lose at least 50% of the possible points and we may not grade them at all.

This assignment is worth about 1% of your grade in the class and is graded out of 30 points. Remember you may drop two assignments (individual or group).

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1. Using standard gates as well as full-adders, design a 6-bit ripple-carry adder with overflow detection. The device should take 2 6-bit inputs "X[5:0]" and "Y[5:0]" and generate the following outputs:
    - The result of the addition, "S[5:0]"
    - If overflow occurred for an unsigned addition, "UO"
    - If overflow occurred for a 2's complement addition, "TO"UO and TO should be 1 iff the addition overflows the associated representation (the 6-bit adder should be easy; the overflow is the hard part here). **[4]**
  2. Design a 4 to 1 MUX in Verilog by first designing a 2 to 1 MUX and then instantiating three 2 to 1 MUXes to build the 4 to 1 MUX. *Minor* syntax errors will be ignored. **[4]**
  3. Design a 4 to 1 MUX using only tri-state drivers and inverters. **[4]**
  4. Problems 3.2ab and 3.3ab. **[1]**
  5. We saw in the class how an SR latch can be created using NOR gates. It is also possible to create an SR latch using only NAND gates by replacing the NOR gates with NAND gates. Analyze (using truth tables, timing diagrams etc.) this new NAND gate based SR latch. What changes do you need to do to the S and R inputs, to stay compatible with the NOR gate based implementation? **[5]**
  6. Do problems 3.12, and 3.15. Be careful when copying the figures from the book. **[4]**
  7. Problem 3.20. **[4]**

8. Draw the output of this circuit in the given timing diagram. Initial values of Q1, Q0 should be assumed to be 0. Propagation delays of all circuit elements are negligible on the time scale of this trace. [4]

