University of Michigan
EECS 311: Electronic Circuits
Fall 2008

Final Exam

12/12/2008

NAME: _____

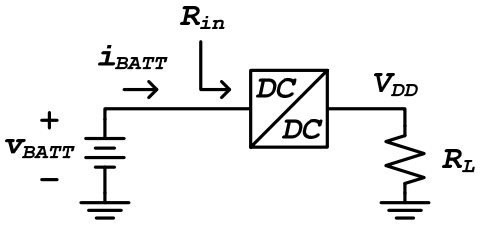
Honor Code:
I have neither given nor received unauthorized aid on this examination, nor have I concealed any violations of the Honor Code.

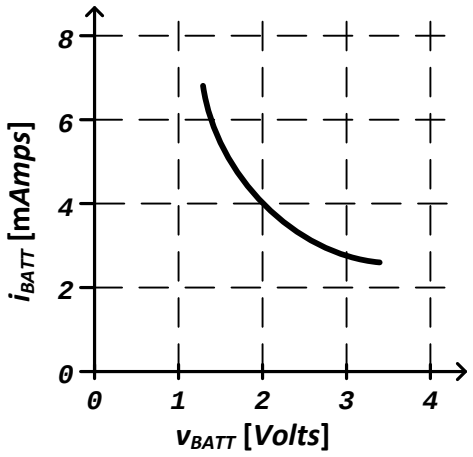
Signature _____

Problem	Points	Score	Initials
1	**25**		
2	**30**		
3	**15**		
4	**30**		
	Total		

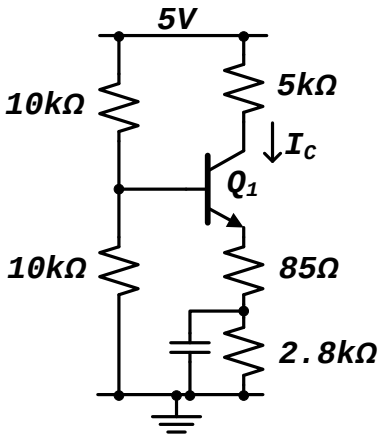
Problem 1 (25 Points): Potpourri – all parts in the problem are unrelated.

a) A DC to DC converter regulates a variable DC voltage source, such as a battery, to a stable voltage source (e.g. V_{DD}). The symbol for a DC/DC converter is shown below, along with a typical response of i_{BATT} vs. v_{BATT}. From the graph, approximate a numerical value for the small-signal input resistance R_{in} in Ohms at a DC operating voltage of $V_{BATT} = 2V$.

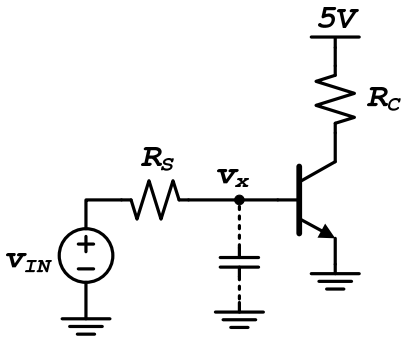




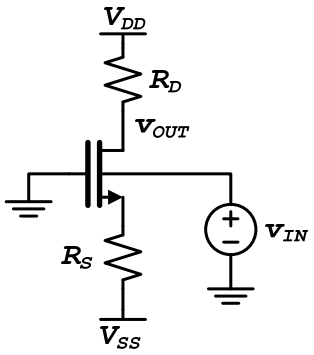
b) Determine the region of operation of Q_1, and find the DC bias current I_C for the following circuit. Assume $\beta_F = 25$, $V_{BE(on)} = 0.5V$, and $V_{CE(sat)} = 0.25V$. Ignore base width modulation.



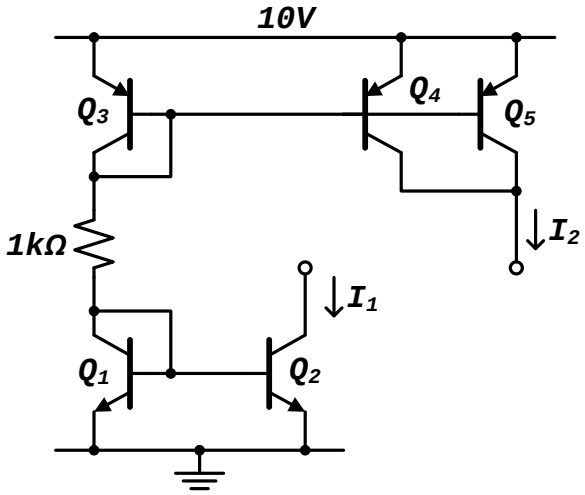
c) You built the following circuit on your breadboard, and measured $B_F = 100$, $g_m = 10m\Omega^{-1}$, $R_C = 10k\Omega$, and $R_S = 10k\Omega$. You measured the small-signal frequency response of v_x/v_{in} which has a DC gain of 0.5, and a 3dB upper cutoff frequency of $160kHz$. You think this cutoff frequency is completely due to Miller multiplication of C_μ. Assuming no other capacitances in the circuit, approximate the value of C_μ. You may neglect base width modulation.



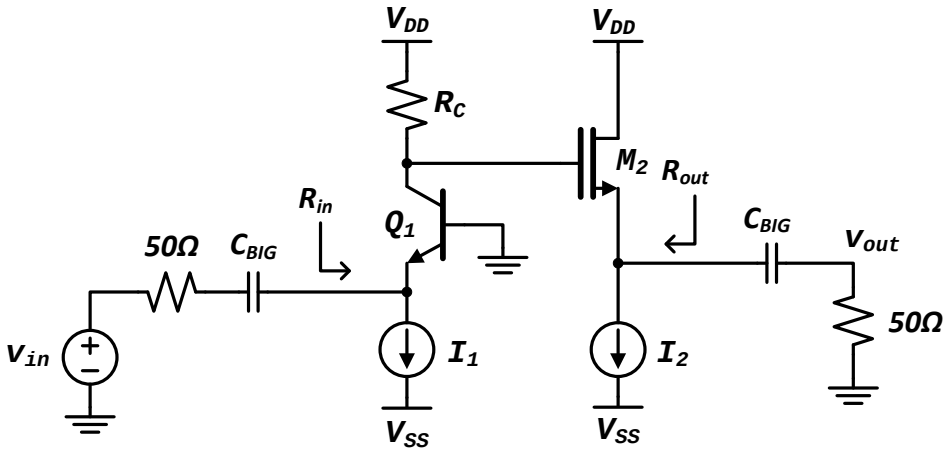
d) Find an expression for the midband gain $A_v = v_{out}/v_{in}$ of the following amplifier in terms of the small signal parameters. The input voltage is applied to the body terminal of the FET. Include body effect in your small signal model. Ignore channel length modulation.



e) Find values for the two output currents I_1 and I_2 for the circuit below. Assume $Q_1 = Q_2$, $Q_3 = Q_4 = Q_5$, and $\beta_F = \infty$. Assume the NPN $V_{BE(on)} = 0.7V$, and the PNP $V_{BE(on)} = -0.7V$, and all devices are in the forward active region. Ignore base width modulation.



Problem 2 (30 Points): In the following two-stage amplifier, for Q_1 assume $\beta_F = 250$ and $V_{th} = 25mV$, ignore base width modulation, and assume it is in the forward active region. For M_2, assume $\mu_n C_{ox}\frac{W}{L} = 1mA/V^2$, ignore channel length modulation and body effect, and assume it is in saturation. Assume capacitors C_{BIG} are DC coupling capacitors.



a) Identify the topology for each stage (C-E, C-C, C-B, C-S, C-D, C-G).

b) Draw the complete low-frequency small-signal model (DC coupling caps are short, high-frequency caps are open). Label each component (other than 50Ω source and load resistors) in terms of R_C, I_1, I_2, β_F, $\mu_n C_{ox}\frac{W}{L}$, and V_{th}. Make sure to express g_m and r_π in terms of these parameters.

c) Find an expression for the input resistance R_{in} in terms of R_C, I_1, I_2, β_F, $\mu_n C_{ox}\frac{W}{L}$, and V_{th}. The definition of R_{in} is shown in the schematic.

d) Solve for the value of I_1 required for an input resistance of $R_{in} = 50\Omega$.

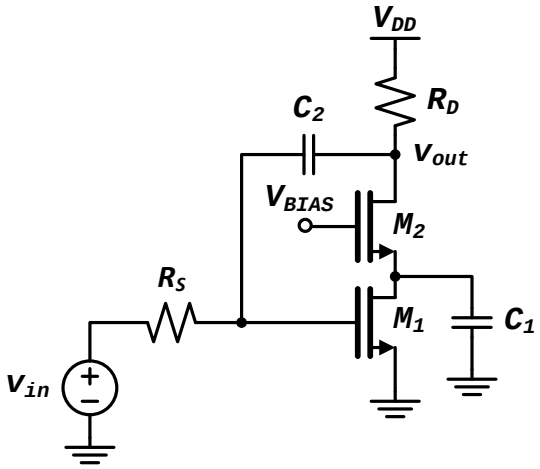
e) Find an expression for the output resistance R_{out} in terms of R_C, I_1, I_2, β_F, $\mu_n C_{ox}\frac{W}{L}$, and V_{th}. The definition of R_{out} is shown in the schematic.

f) Find an expression for midband gain $A_v = v_{out}/v_{in}$ in terms of R_C, I_1, I_2, β_F, $\mu_n C_{ox}\frac{W}{L}$, and V_{th}.

g) Solve for the values of I_2 and R_C that result in an output resistance of $R_{out} = 50\Omega$ and a gain of $A_v = 25$.

h) Assuming $R_{in} = 50\Omega$, $R_{out} = 50\Omega$, and $C_{BIG} = 10\mu F$, use SCTC to find a value for the lower cutoff frequency f_L.

Problem 3 (15 Points): The amplifier shown below is referred to as a Cascode stage. It consists of a common-source stage, followed by a common-gate stage. For the following problem, neglect channel length modulation and body effect, assume both transistors are matched and are biased in the saturation region, assume C_1 and C_2 are high-frequency capacitors, and there are no other high-frequency capacitors in the circuit (neglect C_{gd}, C_{gs},, etc.)

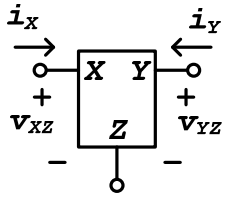


a) Draw the high-frequency small-signal model for the amplifier, including C_1 and C_2.

b) Find an expression for the midband small-signal gain $A_v = v_{out}/v_{in}$, assuming the high-frequency capacitors are open-circuits.

c) Use OCTC to find an expression for the upper cutoff frequency f_H. Apply the Miller multiplication technique across capacitor C_2. For this part, assume $v_{out}/v_{in} = -A$, and leave your answer in terms of A and the other elements in the small-signal circuit.

Problem 4 (30 Points): This problem you will linearize the three-terminal device shown below with terminals X, Y, and Z. Current i_X and i_Y are defined into the device, as shown in the symbol.



The large-signal response for current i_Y is given in the form of an expression as follows:

Large-Signal i_Y: $i_Y = 0.01(v_{XZ})^3$

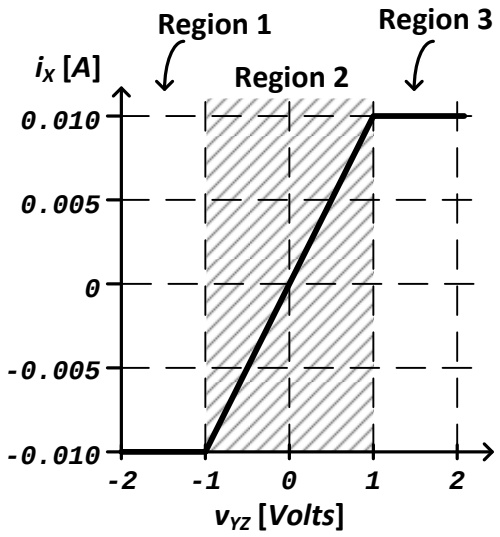
The large-signal response for current i_X is given in the form of a graph, shown below. There are three regions of operation as defined by the inequalities below, and the large-signal current response in each region can be found from the graph.

Definition of regions of operation:

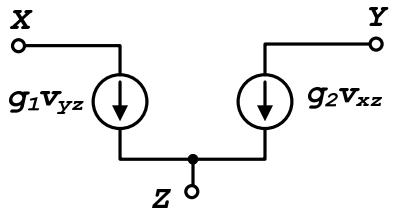
Region 1: $v_{YZ} < -1V$

Region 2: $-1V \leq x_{YZ} \leq 1V$

Region 3: $v_{YZ} > 1V$

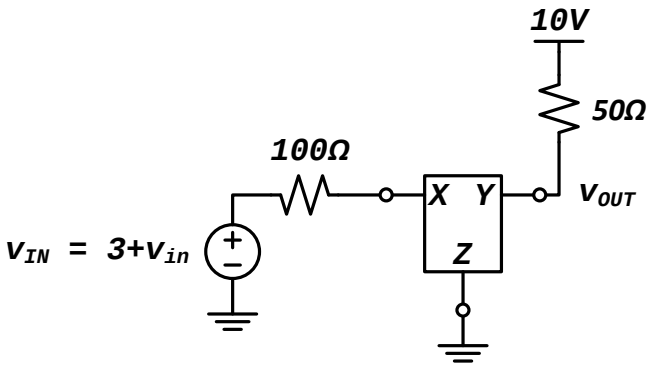


a) The small-signal response of this device can be represented by the model below where g_1 and g_2 are small-signal transconductances with units Ω^{-1}. Which transconductance (g_1 or g_2) represents the linearized i_X and which one represents linearized i_Y?



b) Derive expressions for the transconductances g_1 and g_2 in terms of the DC operating point I_X, I_Y, V_{XZ}, and V_{YZ}. Note that the transconductance representing linearized i_X will have three separate expressions for transconductance; one for each region of operation.

c) Solve for the values for the DC bias voltages V_{XZ} and V_{YZ} at the DC operating point of the circuit below. Note that the input voltage source has a DC bias voltage of $3V$ plus a small-signal input v_{in}.



d) Draw the small-signal circuit for the circuit from part c). Derive an expression for the small-signal gain $A_v = v_{out}/v_{in}$ and evaluate the gain at the DC operating point found in part c).