University of Michigan
EECS 311: Electronic Circuits
Fall 2008

PROBLEM SET 6

Issued 10/22/2008
Due in Lecture 10/29/2008

J&B refers to the course text: "Microelectronic Circuit Design (3rd Edition)," by Richard Jaeger and Travis Blalock.

For the following problems P6.1-P6.6, use the circuit referred to in J&B. For each problem, do the following three parts.

a)   Draw the large-signal DC model of the circuit that you would use to find the DC operating point. All small signal inputs should be zero, and any bypass capacitors are open-circuit. You do not need to solve for the DC operating point.

b)   Draw the small-signal AC model of the circuit that you would use to find the small-signal gain. Replace any active device with its small-signal model. The small signal model may ignore body-effect in FETs, but should include base-width modulation (BJT) or channel-length modulation (FET). At AC, all bypass capacitors should be replaced with a short-circuit. In small-signal, all DC sources are set to zero.

c)   Find the expression for the small-signal gain of the circuit, $a_v = v_{out}/v_{in}$.

P6.1   J&B Figure P13.3

P6.2   J&B Figure P13.3, replace NPN with a NMOS.

P6.3   J&B Figure P13.5

P6.4   J&B Figure P13.5, replace the PNP with a PMOS.

P6.5   J&B Figure P13.6

P6.6   J&B Figure P13.6, replace the NMOS with a NPN.