Honor Code:
I have neither given nor received unauthorized aid on this examination, nor have I concealed any violations of the Honor Code.

Signature ____________________________________________________________________________

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Problem 1 (25 Points): Potpourri – all parts in the problem are unrelated.

a) A DC to DC converter regulates a variable DC voltage source, such as a battery, to a stable voltage source (e.g. $V_{DD}$). The symbol for a DC/DC converter is shown below, along with a typical response of $i_{BATT}$ vs. $v_{BATT}$. From the graph, approximate a numerical value for the small-signal input resistance $R_{in}$ in Ohms at a DC operating voltage of $V_{BATT} = 2V$.

\[
R_{in} = \left( \frac{\partial \Delta i_{BATT}}{\partial \Delta v_{BATT}} \right)^{-1} = \frac{\Delta v_{BATT}}{\Delta i_{BATT}}
\]

\[
= \frac{1V}{-2mA} = \frac{-5000\Omega}{-2mA}
\]
b) Determine the region of operation of $Q_1$, and find the DC bias current $I_C$ for the following circuit. Assume $\beta_F = 25$, $V_{BE(on)} = 0.5V$, and $V_{CE(sat)} = 0.25V$. Ignore base width modulation.

\[
I_C = (5 - 0.25) \frac{1}{SK + SK/2.88SK} - (2.5 - 0.5) \frac{SK/2.88SK}{SK(SK + SK/2.88SK)}
\]

\[
= 0.588 mA
\]
c) You built the following circuit on your breadboard, and measured $B_F = 100$, $g_m = 10m\Omega^{-1}$, $R_C = 10k\Omega$, and $R_S = 10k\Omega$. You measured the small-signal frequency response of $v_x/v_{in}$ which has a DC gain of 0.5, and a 3dB upper cutoff frequency of 160kHz. You think this cutoff frequency is completely due to Miller multiplication of $C_m$. Assuming no other capacitances in the circuit, approximate the value of $C_m$. You may neglect base width modulation.

\[ \frac{v_e}{v_x} = -g_mR_C = -100 \]

\[ R_{o1} = \frac{R_m}{R_S} = 5k\Omega \]

\[ OC TC \quad f_H = \frac{1}{2\pi R_{o1} C_m} \]

\[ C_m = 200pF \]

\[ C_m = C_m (1 + A) = C_m (1 + 100) \]

\[ C_m = 1.97pF \]
d) Find an expression for the midband gain \( A_v = \frac{v_{out}}{v_{in}} \) of the following amplifier in terms of the small signal parameters. The input voltage is applied to the body terminal of the FET. Include body effect in your small signal model. Ignore channel length modulation.

\[
\frac{v_{out}}{v_{in}} = \frac{-M g_m R_D}{1 + (1+\eta) g_m R_S}
\]
e) Find values for the two output currents $I_1$ and $I_2$ for the circuit below. Assume $Q_1 = Q_2$, $Q_3 = Q_4 = Q_5$, and $\beta_F = \infty$. Assume the NPN $V_{BE(on)} = 0.7\,V$, and the PNP $V_{BE(on)} = -0.7\,V$, and all devices are in the forward active region. Ignore base width modulation.

\[
I_{\text{Ref}} = \frac{10 - 0.7 - 0.7}{1\,k} = 8.6\,\text{mA}
\]

\[
I_1 = I_{\text{Ref}} = 8.6\,\text{mA}
\]

\[
I_2 = 2 \times I_{\text{Ref}} = 17.2\,\text{mA}
\]
Problem 2 (30 Points): In the following two-stage amplifier, for $Q_1$ assume $\beta_F = 250$ and $V_{th} = 25mV$, ignore base width modulation, and assume it is in the forward active region. For $M_2$, assume $\mu n C_{ox} W L = 1mA/V^2$, ignore channel length modulation and body effect, and assume it is in saturation. Assume capacitors $C_{BIG}$ are DC coupling capacitors.

![Diagram of two-stage amplifier](image)

a) Identify the topology for each stage (C-E, C-C, C-B, C-S, C-D, C-G).

Stage 1: C-B  
Stage 2: C-D

b) Draw the complete low-frequency small-signal model (DC coupling caps are short, high-frequency caps are open). Label each component (other than 50Ω source and load resistors) in terms of $R_C, I_1, I_2, \beta_F, \mu n C_{ox} W L$, and $V_{th}$. Make sure to express $g_m$ and $r_n$ in terms of these parameters.

\[
I_C = \frac{\beta}{\beta + 1} I_1, \quad I_D = I_2
\]
c) Find an expression for the input resistance $R_{in}$ in terms of $R_C, I_1, I_2, \beta_F, \mu_n C_{ox} \frac{w}{L}$, and $V_{th}$. The definition of $R_{in}$ is shown in the schematic.

$$R_{in} = R_m + \frac{1}{g_m}$$

$$= \frac{\sqrt{I_F}}{I_1}$$

\[ I_1 = 500 \mu A \]

d) Solve for the value of $I_1$ required for an input resistance of $R_{in} = 50 \Omega$. 
e) Find an expression for the output resistance $R_{out}$ in terms of $R_C, I_1, I_2, \beta_f, \mu_n C_{ox} \frac{W}{L}$, and $V_{th}$.

The definition of $R_{out}$ is shown in the schematic.

\[ R_{out} = \frac{1}{g m_2} = \frac{1}{\sqrt{2 \mu_n C_{ox} \frac{W}{L} I_2}} \]

f) Find an expression for midband gain $A_v = v_{out}/v_{in}$ in terms of $R_C, I_1, I_2, \beta_f, \mu_n C_{ox} \frac{W}{L}$, and $V_{th}$.

\[ A_v = \frac{V_T}{V_T + 50 I_1} \cdot \frac{I_1 \beta R_C}{(\beta+1) V_T} \cdot \frac{1}{1 + 50 \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_2}} \]
g) Solve for the values of $I_2$ and $R_c$ that result in an output resistance of $R_{\text{out}} = 50\Omega$ and a gain of $A_v = 25$.

\[ I_2 = 200\, \text{mA} \]
\[ R_c = 5.02\, \text{k}\Omega \]

h) Assuming $R_{\text{in}} = 50\Omega$, $R_{\text{out}} = 50\Omega$, and $C_{\text{BIG}} = 10\mu F$, use SCTC to find a value for the lower cutoff frequency $f_L$.

\[ R_{S1} = 100\, \Omega \]
\[ R_{S2} = 100\, \Omega \]

\[ f_L = \frac{1}{2\pi} \left( \frac{1}{100 \cdot C_{\text{BIG}}} + \frac{1}{100 \cdot C_{\text{BIG}}} \right) = 318\, \text{Hz} \]
Problem 3 (15 Points): The amplifier shown below is referred to as a Cascode stage. It consists of a common-source stage, followed by a common-gate stage. For the following problem, neglect channel length modulation and body effect, assume both transistors are matched and are biased in the saturation region, assume $C_1$ and $C_2$ are high-frequency capacitors, and there are no other high-frequency capacitors in the circuit (neglect $C_{gd}$, $C_{gs}$, etc.)

![Amplifier Diagram]

a) Draw the high-frequency small-signal model for the amplifier, including $C_1$ and $C_2$. 

![Small-Signal Model Diagram]
b) Find an expression for the midband small-signal gain $A_v = v_{out}/v_{in}$, assuming the high-frequency capacitors are open-circuits.

\[
\frac{v_{out}}{v_{in}} = - g_m R_D
\]
c) Use OCTC to find an expression for the upper cutoff frequency $f_{HI}$. Apply the Miller multiplication technique across capacitor $C_2$. For this part, assume $v_{out}/v_{in} = -A$, and leave your answer in terms of $A$ and the other elements in the small-signal circuit.

\[
F_H = \frac{1}{2\pi} \cdot \frac{1}{R_S C_2 (1+A) + C_1/g_m + C_2 (1+\frac{v}{A}) R_D}
\]
Problem 4 (30 Points): This problem you will linearize the three-terminal device shown below with terminals $X, Y, \text{and} \ Z$. Current $i_X$ and $i_Y$ are defined into the device, as shown in the symbol.

![Device Diagram]

The large-signal response for current $i_Y$ is given in the form of an expression as follows:

**Large-Signal $i_Y$:** \[ i_Y = 0.01(v_{XZ})^3 \]

The large-signal response for current $i_X$ is given in the form of a graph, shown below. There are three regions of operation as defined by the inequalities below, and the large-signal current response in each region can be found from the graph.

**Definition of regions of operation:**

- **Region 1:** \[ v_{YZ} < -1V \]
- **Region 2:** \[ -1V \leq v_{YZ} \leq 1V \]
- **Region 3:** \[ v_{YZ} > 1V \]
a) The small-signal response of this device can be represented by the model below where $g_1$ and $g_2$ are small-signal transconductances with units $\Omega^{-1}$. Which transconductance ($g_1$ or $g_2$) represents the linearized $i_x$ and which one represents linearized $i_y$?

![Diagram of a device with transconductances $g_1$ and $g_2$.]

$g_1$ lin. $i_x$

$g_2$ lin. $i_y$

b) Derive expressions for the transconductances $g_1$ and $g_2$ in terms of the DC operating point $I_x, I_y, V_{xz}$, and $V_{YZ}$. Note that the transconductance representing linearized $i_x$ will have three separate expressions for transconductance; one for each region of operation.

$$g_1 = \left. \frac{d i_x}{d v_{yz}} \right|_{dc \; op}$$

Region 1: $g_1 = 0$

Region 2: $g_1 = 10m\Omega$

Region 3: $g_1 = 0$

$$g_2 = \left. \frac{d u_y}{d v_{xz}} \right|_{dc \; op}$$

$g_2 = 0.03 (V_{xz})^2$
c) Solve for the values for the DC bias voltages $V_{XZ}$ and $V_{YZ}$ at the DC operating point of the circuit below. Note that the input voltage source has a DC bias voltage of $3\text{V}$ plus a small-signal input $v_{in}$.

\[ v_{IN} = 3 + v_{in} \]

\[ v_{OUT} = 10\text{V} \]
\[ 50\Omega \]
\[ 100\Omega \]

\[ V_{XZ} = 3 - i_x 100 \]
\[ V_{YZ} = 10 - 50 i_y \]

\[ i_y = 0.01 V_{XZ}^3 \]
\[ i_x = 10\text{mA} \ (\text{Reg 3}) \]

\[ V_{XZ} = 2\text{V} \]
\[ i_y = 80\text{mA} \]
\[ V_{YZ} = 6\text{V} \]
d) Draw the small-signal circuit for the circuit from part c). Derive an expression for the small-signal gain $A_v = \frac{v_{out}}{v_{in}}$ and evaluate the gain at the DC operating point found in part c).

\[ A_v = -\frac{50g_2}{1 - 5000g_1g_2} \]

at DC op

\[ g_1 = 0 \]
\[ g_2 = 0.12 \]

\[ A_v = -6 \]