**University of Michigan**
**EECS 311: Electronic Circuits**
**Fall 2009**

Final Exam

12/21/2009

NAME: Solutions

**Honor Code:**
I have neither given nor received unauthorized aid on this examination, nor have I concealed any violations of the Honor Code.

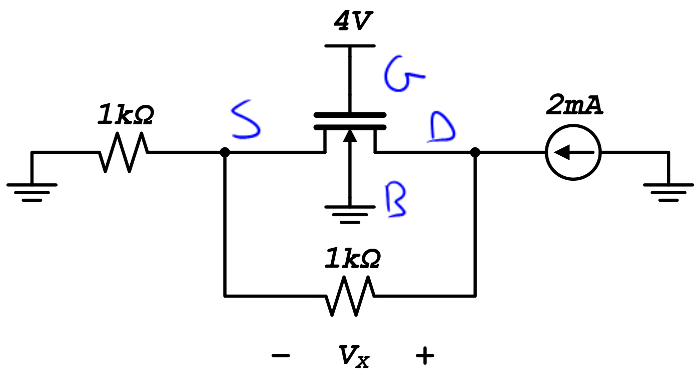
Signature ______________________________________

| Problem | Points | Score | Initials |
|---|---|---|---|
| 1 | 21 | | |
| 2 | 16 | | |
| 3 | 32 | | |
| 4 | 24 | | |
| 5 | 7 | | |
| | Total | | |

**Problem 1 (21 Points):** Potpourri.

a) In the circuit below, label the Source, Drain, Gate, and Body terminals on the NMOS device. Find the region of operation and calculate value of the DC voltage $V_X$. Ignore body-effect.

| |
|---|
| $K_N = \mu_N C_{ox} W/L = 1mA/V^2$ |
| $V_{TN} = 1V$ |
| $\lambda = 0$ |




$V_S = 2V$

$V_{GS} = 2V$

Sat $I_D = \frac{1}{2} K_n (V_{GS} - V_{TN})^2 = 0.5mA$

$I_{RX} = 2m - 0.5m = 1.5mA$

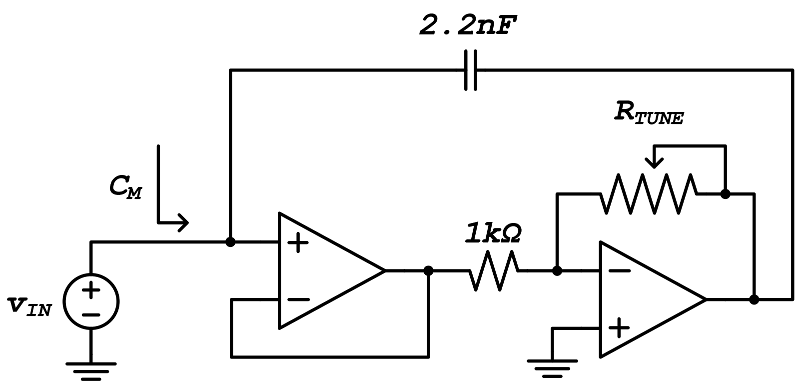
$V_X = 1.5V$

Label Source, Gate, Drain, and Body terminals on the FET above.

Region of operation: Sat

$V_X$ = 1.5

b) You need to build a variable capacitor, but only have the components in the 311 lab to work with. You came up with the topology below, which you think will provide a variable capacitance value $C_M$ at the input due to Miller multiplication. $C_M$ is varied by a potentiometer connected such that it can vary the value of feedback resistance $R_{TUNE}$. Now you need to pick a tuning range for $R_{TUNE}$. Using the Miller effect, calculate value $R_{TUNE}$ should be to achieve a maximum $C_M$ of $100nF$. Assume ideal opamps.




$$A_v = -\frac{R_{TUNE}}{1K}$$

$$C_M = 2.2nF\left(1 + \frac{R_{TUNE}}{1K}\right) = 100nF$$

$$R_{TUNE} = 44.5K$$

Value of $R_{TUNE}$ for $C_M = 100nF$ = $44.5k\Omega$

c) Below are 2 plots taken from the datasheet for an opamp manufactured by Analog Devices. From these plots, approximate the gain-bandwidth product and the slew rate of the opamp.

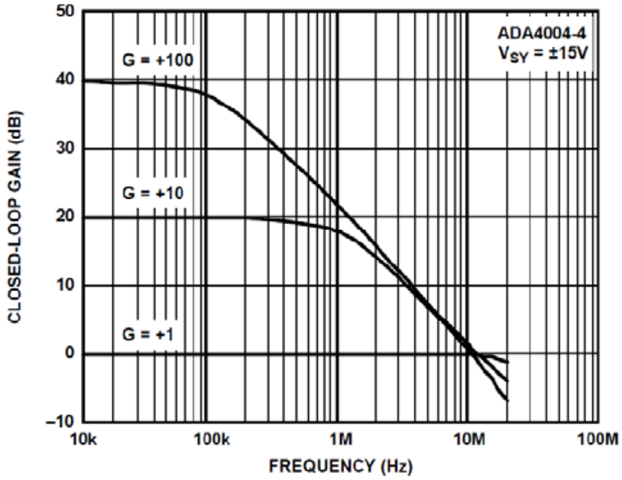



*Figure 21. Closed-Loop Gain vs. Frequency*

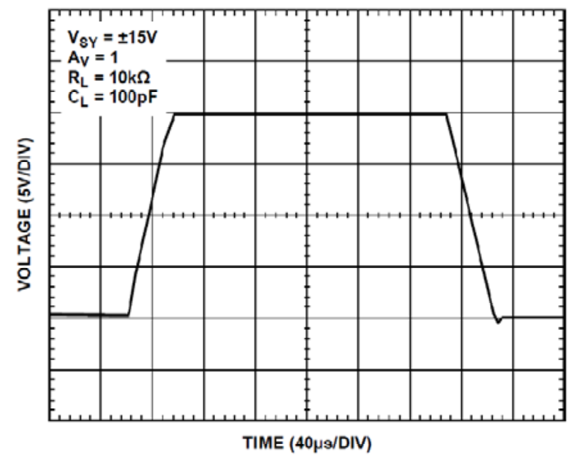
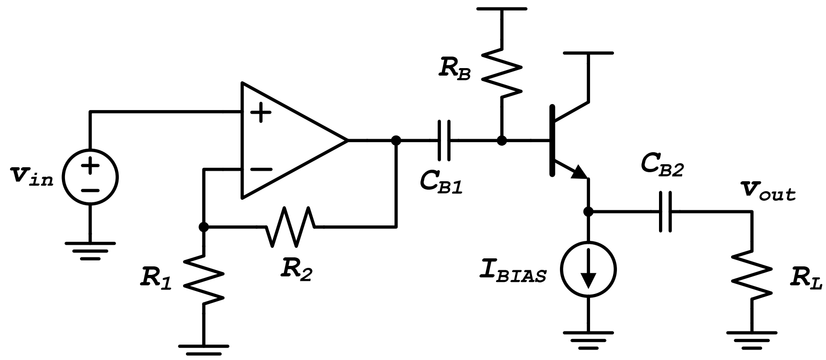



*Figure 28. Large-Signal Transient Response*

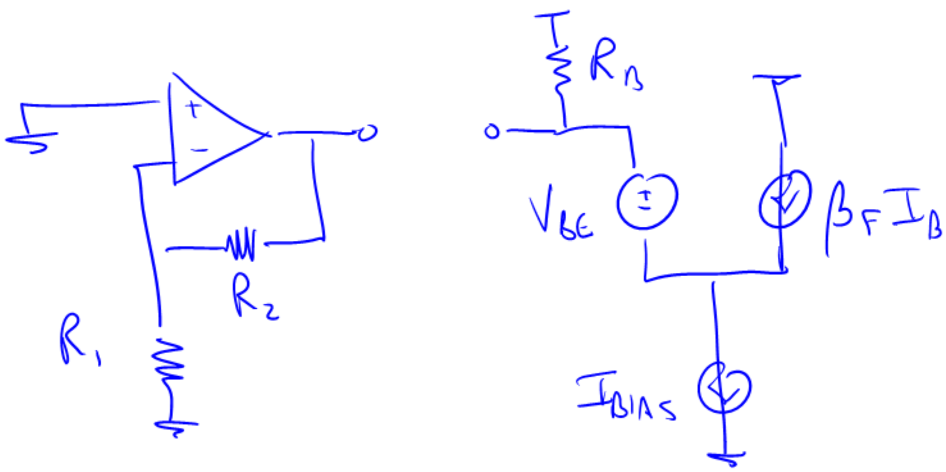
Gain-Bandwidth Product: 10 M

Slew Rate: 0.5 V/μs

**Problem 2 (16 Points):** For this problem, use the circuit below assuming the opamp is linear and ideal, the DC value of $V_{IN} = 0$, ignore $r_o$, and $C_{B1}$ and $C_{B2}$ are bypass capacitors.




a) Draw the DC (large-signal) circuit, assuming the BJT is in FAR and using the constant-voltage drop model.



b) Use the SCTC method to find an expression for the lower cutoff frequency, $\omega_L$. Capacitors $C_{B1}$ and $C_{B2}$ are bypass capacitors.

$C_{B1}$:

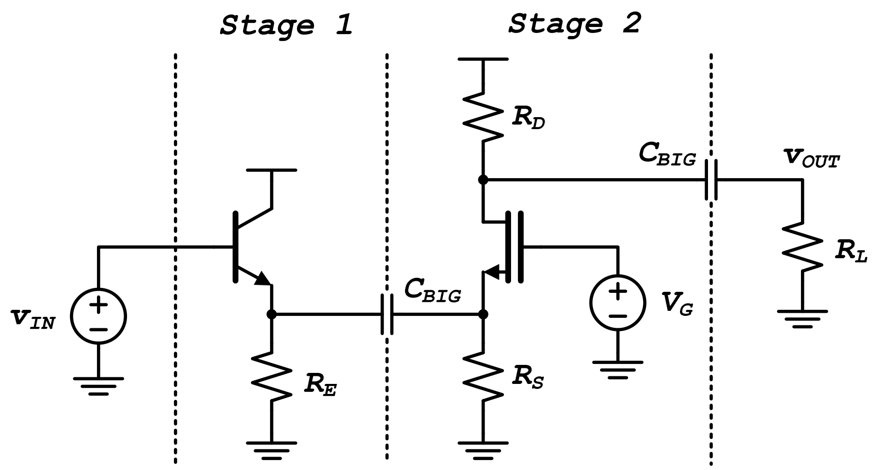
$$R_{B1} = R_B \,||\, (r_\pi + R_L + g_m r_\pi R_L)$$

$C_{B2}$:

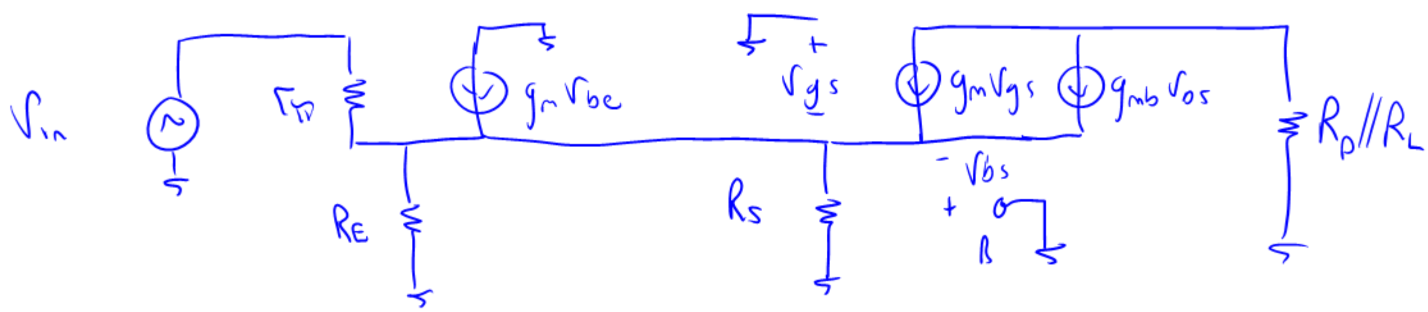
$$R_{B2} = R_L + \frac{1}{g_m} \,||\, r_\pi$$

$$\omega_L = \frac{1}{R_{B1} C_{B1}} + \frac{1}{R_{B2} C_{B2}}$$

**Problem 3 (32 Points):** Use the following two-stage amplifier for this problem. The stages are separated by the dashed lines. Assume the BJT is biased in FAR, and the FET is biased in Sat. For all parts, ignore $r_o$ for both transistors and include $g_{mb}$.




a) Draw the complete small-signal circuit for the amplifier.



b) Find expressions for $R_{in}$, $R_{out}$, and $G_m$ for Stage 1, as indicted by the dashed lines. Ignore $r_o$ for both transistors, and include $g_{mb}$.

$R_{in1}$ = $r_\pi + \left(R_E \| R_S \| \frac{1}{(\eta+1)g_m}\right)(1 + g_m r_\pi)$

$R_{out1}$ = $R_E \| r_\pi \| 1/g_m$

$G_{m1}$ = $-(g_m + 1/r_\pi)$

c) Find expressions for $R_{in}$, $R_{out}$, and $G_m$ for Stage 2, as indicted by the dashed lines. Ignore $r_o$ for both transistors, and include $g_{mb}$.

$R_{in2}$ = $R_S \parallel \frac{1}{(\eta+1)g_m}$

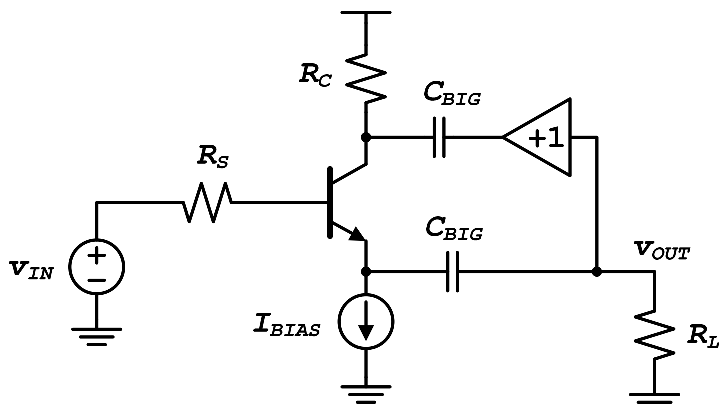
$R_{out2}$ = $R_D$

$G_{m2}$ = $-(g_m + g_{mb})$

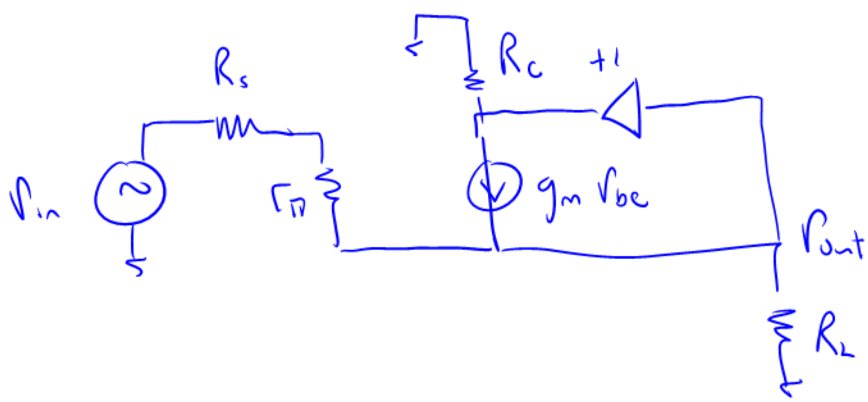
d) Find an expression for the overall gain of the amplifier, $v_{out}/v_{in}$. You may leave your answer in terms of $R_{in}$, $R_{out}$, and $G_m$ of the two stages.

$v_{out}/v_{in} =$ $G_{m1} G_{m2} (R_{out1} || R_{in2}) (R_{out2} || R_L)$

**Problem 4 (24 Points):** The following circuit is called a "bootstrapped" buffer, where the output signal is fed back to the collector of an emitter-follower stage with a gain of +1. This bootstrapping is used to increase the bandwidth of the buffer. For this problem, assume the feedback amplifier with gain of +1 is linear and ideal ($R_{in} = \infty$, $R_{out} = 0$, $v_o/v_i = 1$), the BJT is biased in the FAR region, you can ignore $r_o$, and $C_{BIG}$ is a bypass capacitor.




a) Draw the small-signal circuit for the buffer. Ignore $r_o$.



b) Find and expression for the mid-band small-signal gain, $a_v = v_{out}/v_{in}$. Ignore $r_o$.

$$\frac{v_o}{v_x} = \frac{R_L(1+g_m r_\pi)}{\underbrace{r_\pi + R_L + g_m r_\pi R_L}_{R_{IN}}}$$

$$\frac{v_o}{v_{in}} = \frac{R_{in}}{R_s+R_{in}} \cdot \frac{v_o}{v_x} = \frac{R_L(1+g_m r_\pi)}{R_s + r_\pi + R_L(1+g_m r_\pi)}$$

c) Assume $C_\pi$ and $C_\mu$ are the only high-frequency capacitors in the circuit. Use the OCTC method to find an expression for the upper cutoff frequency, $\omega_H$. Ignore $r_o$.

$C_\mu$:

$$R_{o\mu} = \frac{R_s r_\pi}{R_s + r_\pi + R_L(1 + g_m r_\pi)}$$

$C_\pi$:

$$R_{o\pi} = r_\pi \,//\, \frac{R_L + R_s}{1 + g_m R_L}$$

$$\omega_H = \frac{1}{R_{o\pi} C_\pi + R_{o\mu} C_\mu}$$

**Problem 5 (7 Points):** Multiple choice. Circle only one answer for each part.

a) Which topology has higher input resistance considering equal DC bias currents?

C-E | C-C | About the same

b) Which topology has smaller output resistance, considering $1mA$ DC bias currents at room temperature with $K_N = 1mA/V^2$?

C-C | C-D | About the same

c) Which topology typically has higher gain, considering equal bias current?

C-E | C-B | About the same

d) Which topology typically has higher bandwidth, considering equal bias current?

C-S | C-D | About the same

e) Which topology would you use for a high-gain stage?

C-C | C-E | Both | None

f) If bias current in a C-E amplifier is doubled with the same transistor and collector resistor value, then the gain would:

Double | More than double | Less then double | Stay the same

g) If bias current in a C-S amplifier is doubled with the same transistor and drain resistor value, then the gain would:

Double | More than double | Less then double | Stay the same

(Space for additional work)