University of Michigan
EECS 311: Electronic Circuits
Fall 2009

Quiz 1

10/21/2008

NAME: Solutions

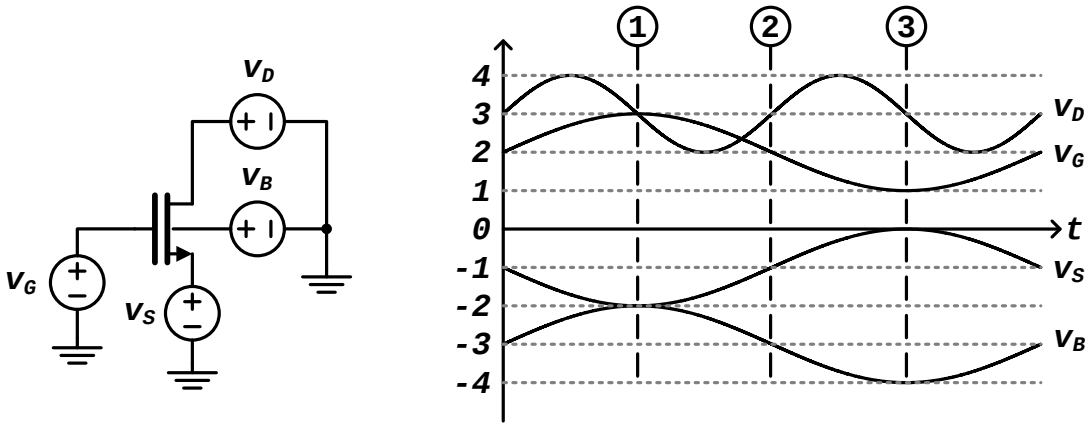
Honor Code:
I have neither given nor received unauthorized aid on this examination, nor have I concealed any violations of the Honor Code.

Signature _____

Problem	Points	Score	Initials
1	**25**		
2	**30**		
3	**15**		
4	**30**		
	Total		

Problem 1 (25 Points): Potpourri – the following problem has three unrelated parts.

a) Use the circuit below for this part, where the voltages applied to the terminals of the NMOS vary with time as shown in the graph. Complete the table below by evaluating the specified voltages and determining the region of operation at the 3 points in time indicated on the graph. Assume for the NMOS that $V_{t0} = 0.5V$, $2\phi_F = 0.5V$, and $\gamma = 0.5V^{1/2}$.



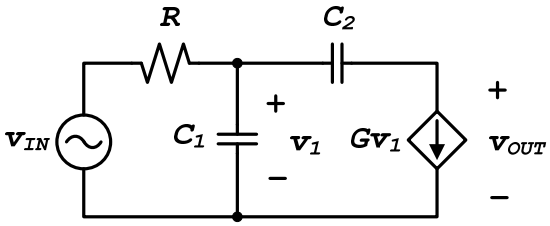
① $V_{SB} = 0$ $\quad V_{tn} = 0.5V$

② $V_{SB} = 2$ $\quad V_{tn} = 0.5 + 0.5\left(\sqrt{2.5} - \sqrt{0.5}\right)$

③ $V_{SB} = 4$ $\quad V_{tn} = 0.5 + 0.5\left(\sqrt{4.5} - \sqrt{0.5}\right)$

Point	v_{GS}	v_{DS}	V_{tn}	Region of Operation
1	5	5	0.5	Sat
2	3	4	0.94	Sat
3	1	3	1.21	Cutoff

b) Find the transfer function $H(s) = v_{OUT}/v_{IN}$ of the following circuit.



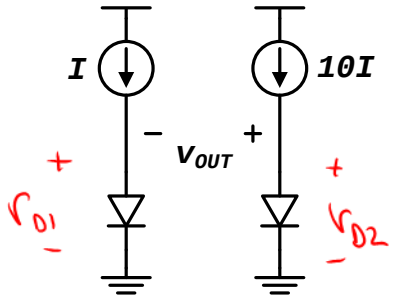
$$\cancel{R}\left(\frac{V_{IN}-V_1}{\cancel{R}}\right) = \left(V_1 s C_1 + G V_1\right) R$$

$$V_1 = V_{IN}\,\frac{1}{1 + sRC_1 + RG}$$

$$V_{OUT} = V_1 - G V_1 \frac{1}{sC_2}$$

$$\boxed{\frac{V_{out}}{V_{IN}} = \frac{1 - \frac{G}{sC_2}}{1 + sRC_1 + GR}}$$

c) Use the circuit below for this part. Assume the two diodes have identical parameters (same I_S and n), and are in the forward bias region. Using the appropriate large-signal model for the diodes, calculate the value for v_{OUT} at a temperature of 100 °C.
$k = 1.38 \cdot 10^{-23}\ J/K$ and $q = 1.6 \cdot 10^{-19}\ C$.



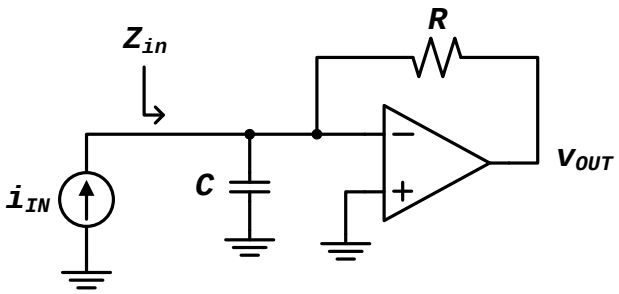
$$v_{D1} \simeq V_T \ln \frac{I}{I_S}$$

$$v_{D2} \simeq V_T \ln \frac{10I}{I_S}$$

$$v_{OUT} = v_{D2} - v_{D1} = V_T \ln\left(\frac{10I}{I_S} \cdot \frac{I_S}{I}\right)$$

$$\boxed{v_{OUT} = V_T \ln 10 = 74\,mV}$$

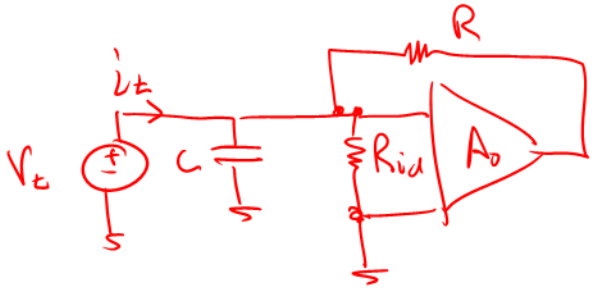
Problem 2 (30 Points): Use the following circuit for all parts of this problem.



a) Assume the opamp has finite gain A_0 and differential input resistance R_{id} between the (+) and (−) terminals. All other parameters of the opamp are ideal. Find an expression for the input impedance Z_{in}.

Apply V_t at input

$$Z_{IN} = \frac{V_t}{i_t}$$



$$i_t = \frac{V_t}{1/sC} + \frac{V_t}{R_{id}} + \frac{V_t - V_{out}}{R}$$

$$V_{id} = -V_t \qquad V_{out} = -A_0 V_t$$

$$i_t = V_t\left(sC + \frac{1}{R_{id}} + \frac{A_0+1}{R}\right)$$

$$Z_{IN} = \frac{1}{sC + \frac{1}{R_{id}} + \frac{A_0+1}{R}}$$

b) Assume the opamp has finite gain and bandwidth, given by the following expression. All other parameters of the opamp are ideal.

$$A(s) = \frac{A_0}{1 + s/\omega_p}$$

Find an expression for the transfer function $H(s) = v_{OUT}/i_{IN}$.

$V_{out} = A(s) V_{i1}$ $\quad V_1 = -V_{i1}$ (V1 @ inv. terminal)

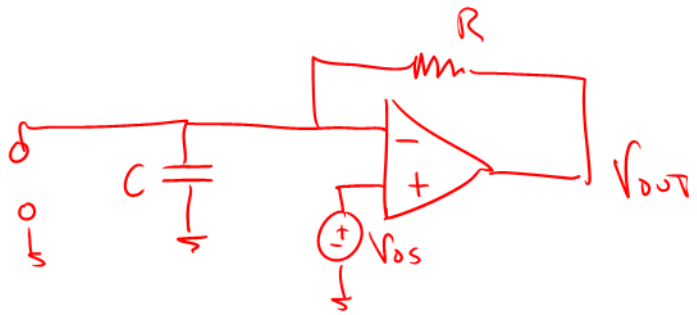
$$i_{IN} = V_1 sC + \frac{V_1 - V_{out}}{R}$$

$$= -V_{out}\left(\frac{sC}{A(s)} + \frac{\frac{1}{A(s)} + 1}{R}\right)$$

$$\frac{V_{out}}{i_{IN}} = -\frac{A(s)R}{1 + sRC + A(s)} \qquad A(s) = \frac{A_0}{1 + s/\omega_p}$$

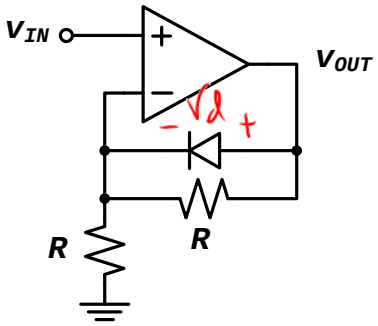
$$\boxed{\frac{V_{out}}{i_{IN}} = -\frac{RA_0}{(sRC+1)(1 + s/\omega_p) + A_0}}$$

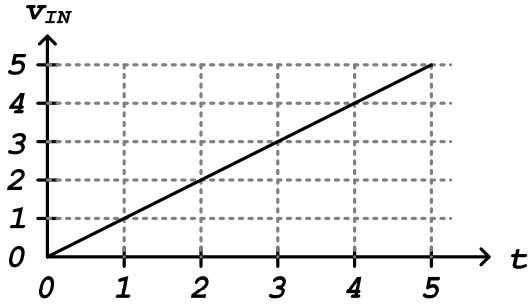
c) Assume the opamp has finite offset voltage V_{OS}. Find an expression for the transfer function $H(s) = v_{OUT}/V_{OS}$ when $i_{IN} = 0$.



$$\frac{V_{out}}{V_{in}} = 1 + \frac{R}{1/sC} = 1 + sRC$$

Problem 3 (15 Points): Use the following circuit for this problem. Assume the opamp is ideal, and use the constant-voltage-drop (CVD) model for the diode with $V_{ON} = 1\ V$. Plot the output voltage v_{OUT} on the graph provided below for an input voltage v_{IN} of a ramp from 0 to $5\ V$ as shown on the graph below.





$V_{IN} < 1$

$V_d = V_{out} \frac{R}{R+R} = \frac{V_{out}}{2}$

$V_{out} = 2 V_{IN}$

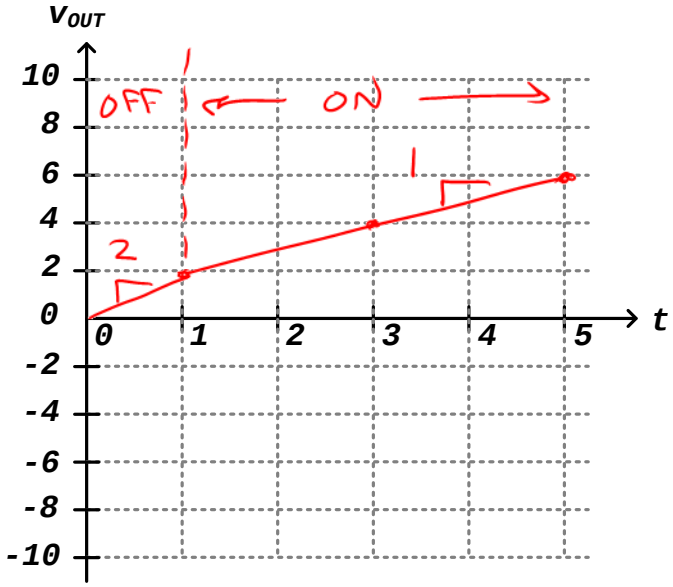
$V_d < 1V$ off

$V_{IN} > 1$

Diode on

$V_{out} = V_{IN} + V_{ON} > 2$

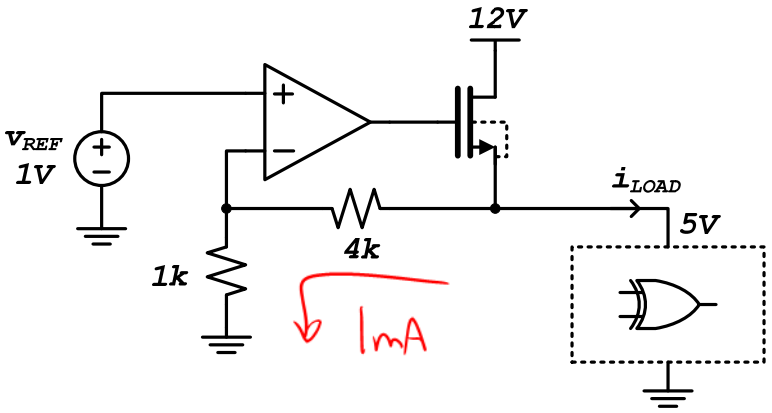
$i_0 = \frac{V_{out} - V_{ON}}{R} - \frac{V_{ON}}{R} > 0$ ✓



Problem 4 (30 Points): Use the parameters from the table below for all parts of this problem. Assume $v_{SB} = 0V$ unless otherwise shown.

	NMOS	PMOS
V_{th}	$1V$	$-1V$
$K_{n,p}$	$500\ \mu A/V^2$	$250\ \mu A/V^2$
$\lambda_{n,p}$	0	0

a) The following circuit is a linear voltage regulator providing a constant $5V$ supply voltage to a digital logic chip. Assuming the NMOS is in the Saturation region, calculate the value of v_{GS} of the NMOS when $i_{LOAD} = 1mA$.

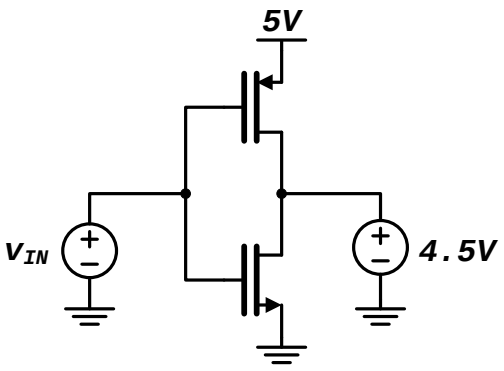


$i_D = 2\,mA$

Sat $\quad i_D = \frac{1}{2} k_n (V_{GS} - V_{tn})^2 = 2mA$

$$\boxed{V_{GS} = 3.83\,V}$$

b) For the circuit below, find the range of v_{IN} that will simultaneously bias the NMOS in the Saturation region, and the PMOS in the Linear region.



NMOS Sat

$V_{GS} - V_{tn} < V_{DS}$

$V_{DS} = 4.5 \quad V_{tn} = 1 \quad V_{GS} = V_{IN}$

$V_{IN} < 5.5\,V$

$V_{GS} > V_{tn}$ & $V_{IN} > 1\,V$

PMOS Linear:

$V_{GS} = V_{IN} - 5$

$V_{DS} = 4.5 - 5 = -0.5V$

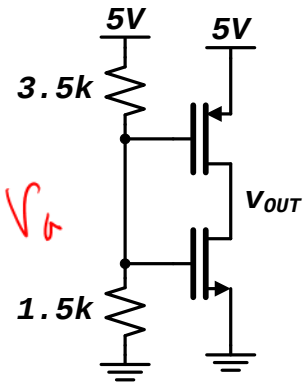
$V_{GS} - V_{tp} < V_{DS} \qquad V_{IN} - 5 + 1 < -0.5$

$V_{IN} < 3.5$

$V_{GS} < V_{pt}$ & $V_{GS} < 4V$

$1V < V_{IN} < 3.5V$

c) For the circuit below, assume the NMOS is in the Saturation region, and the PMOS is in the Linear region. Additionally, approximate the PMOS in Linear with the voltage-controlled resistor model R_{DS} (good for small v_{DS}). Calculate the value for the voltage v_{OUT}.



$V_G = \frac{1.5k}{5k} \cdot 5V = 1.5V$

PMOS Linear

NMOS Sat

$V_{GS}\,(NMOS) = 1.5V$

$V_{GS}\,(PMOS) = 1.5 - 5 = -3.5V$

$i_D = \frac{1}{2} \cdot 0.5m(1.5-1)^2 = \frac{1}{16}\,mA$

$i_D \cdot R_{DS} = \frac{1}{4}\cancel{16}\,m \cdot \frac{1}{\frac{1}{4}m|-3.5+1|} = 0.1V$

$V_{out} = 5 - i_D R_{DS} = 4.9V$

(Space for additional work)