University of Michigan
EECS 311: Electronic Circuits
Fall 2009

LAB 4 – SINGLE-STAGE AMPLIFIER

Issued 11/9/2008
Report due in Lecture 11/23/2008

Introduction

In this lab you will characterize a 2N3904 NPN transistor, and then design a single-stage common-emitter amplifier meeting the specifications given in Table 1 through hand-calculation and Cadence simulation. You will then construct the amplifier in the lab and measure its performance.

Specification	Value
Mid-band Voltage Gain	$\lvert v_o/v_s \rvert \geq 150$
Upper 3dB Cutoff Frequency	$f_H \geq 150\ kHz$
Lower 3dB Cutoff Frequency	$f_L \leq 1kHz$
Maximum Output Voltage Swing	$v_{o(max)} \geq 3\ V_{ppk}$
Source Resistance	$R_S = 830\ \Omega$
Power Supply	$12\ V$
Power Consumption	$10\ mW$
Maximum Capacitor Size	$10\mu F$
DC Bias Point Stability	$R_1 \| R_2 \leq \beta_F R_E/10$

Table 1. Single-stage amplifier specifications.

There is no prelab report due for this lab; however, this is a time consuming lab that requires in-lab measurements be made during both weeks. Your goal should be to have the characterization of the 2N3904, and all design and Cadence simulation completed by the beginning of Week 2 of this lab. Each student must do their own separate design of the amplifier. In lab, you may choose one design (yours or your partners) to build and measure.

Week 1 In-Lab Component – Characterize a 2N3904

P4.1 In this step you will characterize a 2N3904 NPN transistor; therefore, this step must be completed in the lab. The measurements from the NPN will be used in the design of the single stage amplifier in the following steps.

a) Pick a 2N3904 from the general supply in lab. Using the HP4155 Parameter Analyzer, load the *PNPN1* measurement program. Follow the instructions given in the online tutorial for the HP4155.

http://www.eecs.umich.edu/courses/eecs311/f09/tutorials/hp4155.html

Change the sweep range for V_{CE} from 0 to 12V in steps of 0.2V. You must choose the sweep range for I_B based on the transistor you picked. Choose a range of I_B that results in a sweep of I_C from $100\mu A$ to $5mA$. Pick step sizes of I_B to vary I_C by about $500\mu A$.

Note: It will help to mark your transistor so you can identify it. Ask the GSI for colored "Liquid Paper" to put a dot on the top of the transistor.

b) Once the sweep has completed (this will be a long sweep), measure β_F and V_A for the curve with I_C closest to 1mA. Record these values in your lab report template.

c) Save the IB, IC, and VCE variables to files using the *HP4155 Read Data* virtual instrument (VI) for LabVIEW. Follow the instructions on the HP4155 tutorial page on how to download the VI and save this data.

http://www.eecs.umich.edu/courses/eecs311/f09/tutorials/hp4155.html

d) Use the HP4275A to measure C_μ of your 2N3904. Follow the instructions on the following site to measure C_μ.

http://www.eecs.umich.edu/courses/eecs311/f09/tutorials/hp4275a.html

Measure the Base-to-Collector capacitance with the Emitter open-circuited. Apply a reverse bias to the B-C junction of 0V to 12V in steps of 2V. Record these values in your lab report template.

Modeling 2N3904 in Cadence

P4.2 In this step you will develop an NPN model file that matches the 2N3904 you characterized in lab. You will change three values in the template model file, which are Bf, Vaf, and Cjc.

a) Download the *lab4.mod* model file and save it to your Cadence working directory (~/eecs311_f09). This model file will serve as a template.

http://www.eecs.umich.edu/courses/eecs311/f09/labs/lab4.mod

b) Edit the values of *Bf* and *Vaf* in the *lab4.mod* file, changing them to the values of β_F and V_A measured in P4.1 b). Alternatively, if you have measured β_F and V_A at a bias point closer to your chosen DC bias point, you may use that instead.

c) The base-to-collector junction capacitance is modeled by the following expression.

$$C_\mu = \frac{\mathrm{Cjc}}{\left(1 + \frac{V_{CB}}{\mathrm{Vjc}}\right)^{Mjc}}$$

The parameters $Vjc = 0.75$ and $Mjc = 0.3085$ are given in the model file. Using your measured values for C_μ at different values of V_{CB}, determine the best fit value for Cjc in the above expression. Enter this value in the *lab4.mod* file.

d) Test your model file: Create a new library in Cadence called *lab4*. Create a new schematic cell view called *test.* Insert an *analogLib > npn* component in the schematic, and under *model name* for the npn enter *lab4_2n3904*. Add *analogLib > vdc* sources wired to the base and collector of the NPN, also ground the emitter. Give the base a voltage of 0.7V, and the collector 5V.

Launch Analog Environment. Under *Setup > Model Libraries …*, click *Browse…* and find your *lab4.mod* file. Click *OK*, *Add*, and *OK*. Run a DC operating point simulation to verify your model is correctly found (simulation will not run otherwise).

Note: You will need to repeat this step of adding the *lab4.mod* model file every time you close and re-open Analog Environment.

Single Stage Amplifier Design

The schematic for the single stage common emitter amplifier is shown in Figure 1. Use only this topology for your design, choosing component values to meet the specifications given in Table 1. The loading of the oscilloscope probe is modeled as a 15pF capacitor and 10MΩ resistor. The load capacitor C_L is an external capacitor added to the circuit.

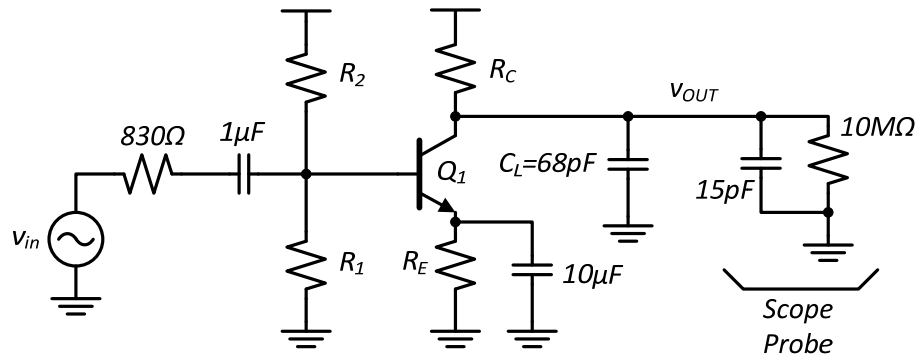

Figure 1. Single-stage amplifier schematic.

P4.3 DC Bias Point: Draw the large-signal circuit at DC and derive an expression relating the bias current I_C to the bias resistors R_1, R_2, and R_E. Assume the constant voltage source model for the B-E junction diode (with what on-voltage?). For simplification, ignore base-width modulation in the NPN. Use this circuit to also find expressions for the power dissipation and maximum output voltage swing V_{oppk}.

P4.4 Hand Design: Draw the small-signal model of the circuit at AC (bypass capacitors C_E and C_B are shorted). Include C_π and C_μ in your NPN model to capture the upper cutoff frequency. Use this circuit to find expressions for the small-signal gain, f_L, and f_H.

Explore the dependencies and trade-offs between the various specs resulting from the expressions you have derived. Using these expressions, and the ones from P4.3, choose a DC operating point and values for all the components to meet the specifications given in Table 1. During the design phase, it may help to ignore base-width modulation or use other simplifications such as $R_1||R_2 \gg r_\pi$ to simplify the problem. Be sure to check these assumptions later on. The amplifier should be completely designed using hand calculations.

P4.5 Cadence Simulation: Simulate your circuit in Cadence using your chosen component values and using the model file created in P4.2. You will have to include the model file each time you launch Analog Environment (refer to P4.2 part d). Simulate the DC, AC, and transient response of the amplifier and verify all specifications are met. Record the simulated values for each specification in the summary table in the lab report.

Week 2 In-Lab Component

L4.1 Build the amplifier. Be careful with polarities of electrolytic capacitors. It will help to add a large decoupling capacitor between V_{DD} and ground of $> 10\mu F$. Use the input stage shown in Figure 2 between the signal generator and your circuit as a 101x attenuator with a source impedance of 830Ω. Note that the attenuation is with respect

to the voltage v_a across the 51Ω resistor (which you should measure with a scope probe), and that the 50Ω resistor is internal to the signal generator. Measure the value of all components in this circuit to calculate the exact attenuation ratio. Connect the output of this circuit to the input of your amplifier. Power your circuit and measure the bias current I_C by measuring the DC voltage drop across R_C.

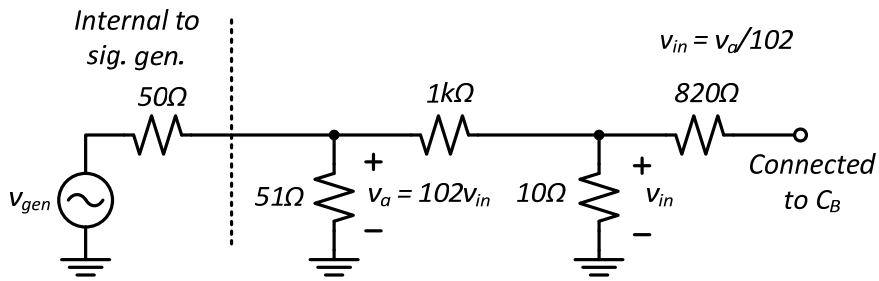

Figure 2. Attenuator circuit with 830Ω source impedance.

L4.2 Apply an input sine wave to your complete circuit through the attenuator in Figure 2 and measure the gain as a function of frequency. The amplitude of the input sine wave should be set to result in an output peak-peak voltage of around 200mV in the midband. Choose a set of frequencies to measure the lower cutoff frequency, mid-band gain and upper cutoff frequency of your amplifier. Record these gains and frequencies in your lab report. Record the exact lower and upper cutoff frequencies (3dB down points), as well as the midband gain. Also measure the power dissipation of the circuit. Show the working circuit to the GSI to get checked off.

L4.3 Apply an input sine wave at a frequency in the midband range and test the maximum peak-peak output voltage swing of the amplifier. With the output waveform displayed on the scope when its peak-peak swing is equal to the specification, save the scope screen to a file using the DSO3000 Scope Connect software. A tutorial to use this software can be found at the link below. Show the working circuit to the GSI to get checked off.

http://www.eecs.umich.edu/courses/eecs311/f09/tutorials/dso3000.html

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LAB 4 – CHECK-OFF SHEET

NAME: _____ LAB SECTION: _____

Have the GSI check you off on the following exercises after you have completed them. Be prepared to answer questions about your circuit or the results.

Exercise ..... Date Completed

P4.1 Show model of 2N3904 (lab4.mod file) ..... _____

P4.4 Show small-signal expressions ..... _____

P4.5 Show printout of AC Cadence response of amplifier ..... _____

L4.2 Mid-band gain, f_L, and f_H specs met ..... _____

L4.3 Maximum output swing spec met ..... _____

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LAB 4 – REPORT TEMPLATE

NAME: _____ LAB SECTION: _____

Use the following lab report template to record your measurements. Use the space provided to answer questions.

Lab Report Template

Parameter	Spec	Hand-Design	Simulation	Measured	Units
$\lvert v_o/v_s \rvert$	≥ 150				V/V
f_H	$\geq 150\ kHz$				kHz
f_L	$\leq 1kHz$				kHz
P_{diss}	$\leq 100\ mW$				mW
V_{out} Swing	$\geq 3\ V_{ppk}$				V
R_1	n/a				kΩ
R_2	n/a				kΩ
R_E	n/a				kΩ
R_C	n/a				kΩ
C_B	$\leq 10\mu F$				µF
C_E	$\leq 10\mu F$				µF

Table 2. Results summary table.

P4.1-2 Enter the following values from the characterization of the 2N3904.

$\beta_F =$ _____ $V_A =$ _____

V_{CB}	C_μ	V_{CB}	C_μ
0 V		8 V	
2 V		10 V	
4 V		12 V	
6 V			

$C_{jc} =$ _____ (value used in lab4.mod)

When determining C_{jc}, was there a large variation in the value calculated from the measured C_μ and explain how you arrived at this value.

P4.4 Draw the small-signal model of the amplifier and summarize your hand calculations below that were used to determine specifications.

Small-signal AC circuit for amplifier:

Small-signal expressions:

v_o/v_{in} = _____

f_H (from OCTC) = _____

f_L (from SCTC) = _____

P4.4 In the space below, explain how you met the maximum output voltage swing requirement.

P4.4 Enter the value of I_C and V_{CE} chosen for your amplifier and calculate the values of the small-signal parameters of the BJT.

I_C = _____ V_{CE} = _____

Parameter	Value	Units
r_π		
r_o		
g_m		
C_π		
C_μ		

In the space below, explain your design methodology for the amplifier in choosing this value of bias current and the other component values. Did you target gain first? Cutoff frequencies? Did you try to optimize for any specification (minimum power or max gain)? Briefly explain below.

L4.1 Measured bias current.

I_C = _____

L4.2 Enter values for your hand-calculated small-signal gain and measured gain below.

Hand calc midband: v_o/v_{in} = _____

Measured midband: v_o/v_{in} = _____

If these values were off my more than 5%, what would you change in your circuit to correct the gain and what other specifications would changing this parameter also affect?

Measured: f_L = _____

Measured: f_H = _____

Use the following table to record measurements of gain over the range of frequencies you choose for your amplifier.

Frequency	v_{inppk}	v_{outppk}	**Frequency**	v_{inppk}	v_{outppk}

L4.3 Sketch the output waveform at $3V_{ppk}$ in the space below, or use the DSO3000 Scope Connect utility to capture the scope screen to a file.

http://www.eecs.umich.edu/courses/eecs311/f08/tutorials/dso3000.html

S4.1 Include the following plots with your lab report and indicate on each plot what it is.

a) Matlab plot of I_C vs. V_{CE} for each value of I_B from importing saved data from HP4155.

b) Cadence AC simulation from 10Hz to 10MHz labeling lower and upper cutoff frequencies as well as midband gain. Plot should be either gain in dB on a log frequency scale, or gain (not in dB) vs. frequency on a log-log scale plot.

c) Plot of the measured gain as a function of frequency of the amplifier (using Matlab, Excel). Take sufficient points to capture f_L, f_H, and the midband gain. Plot the gain on a log-log scale and label all important features on the plot.