University of Michigan
EECS 311: Electronic Circuits
Fall 2009

PROBLEM SET 5

Issued 10/7/2009
Due in Lecture 10/14/2009

J&B refers to the course text: "Microelectronic Circuit Design (3rd Edition)," by Richard Jaeger and Travis Blalock.

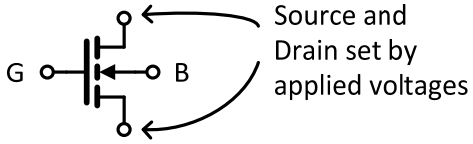
P5.0 Complete the midterm course evaluation available online by logging into **CTools** and following the **Teaching Questionnaires** link. This is completely anonymous (even though you've logged in through CTools), and very valuable to me for making changes to the class while you're still taking it.

The deadline for submitting your evaluation is **Oct. 16**.

P5.1 J&B Problem 4.10.

P5.2 J&B Problem 4.11.

Note: the symbol in these figures represents an NMOS transistor, and the S and D terminals are defined by the voltages applied to the NMOS ($v_S < v_D$).



P5.3 J&B Problem 4.15.

P5.4 J&B Problem 4.23.

P5.5 J&B Problem 4.32.

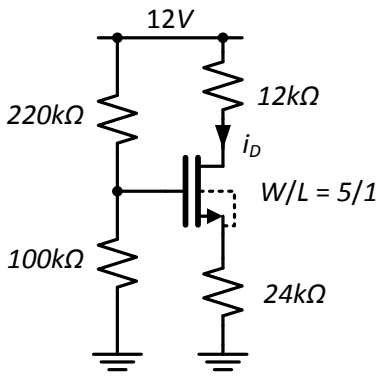
P5.6 J&B Problem 4.43. Ignore channel length modulation ($\lambda = 0$).

P5.7 J&B Problem 4.49. Ignore channel length modulation ($\lambda = 0$).

P5.8 J&B Problem 4.53.

(Additional problems on back)

P5.9 Find the DC bias current i_D through the NMOS transistor. Assume $V_{TN} = 1V$, $\lambda = 0$, and $\mu_n C_{ox} = K_n' = 100\mu A/V^2$.



P5.10 Choose values for R_1 and R_2 so that the DC bias current through the PMOS transistor is $i_D = 100\mu A$, and the current through the biasing branch $i_{R1} = i_{R2} = 10\mu A$. Assume $V_{TP} = -1V$, $\lambda = 0$, and $\mu_p C_{ox} = K_p' = 40\mu A/V^2$.