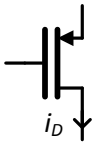
University of Michigan
EECS 311: Electronic Circuits
Fall 2009

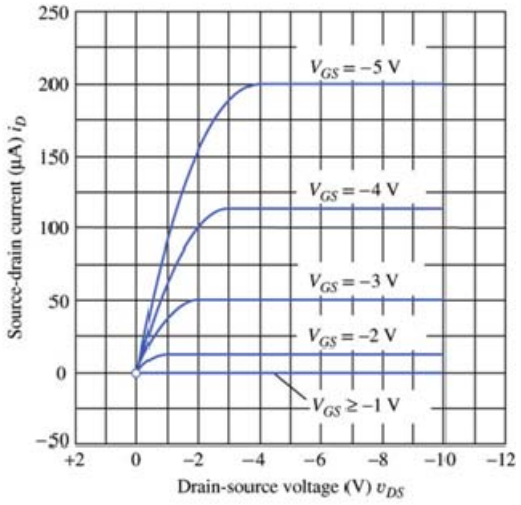
PROBLEM SET 7

Issued 10/28/2009
Due in Lecture 11/4/2009

J&B refers to the course text: "Microelectronic Circuit Design (3rd Edition)," by Richard Jaeger and Travis Blalock.

P7.1 The i_D vs. v_{DS} curves are given to the right for a PMOS device. Estimate the threshold voltage V_{tp} and K_p for the device. Assume $\lambda = 0$ and $v_{BS} = 0$.



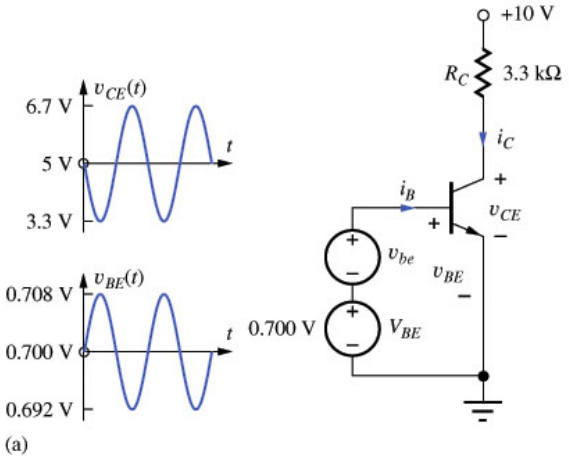


P7.2 J&B Problem 4.54

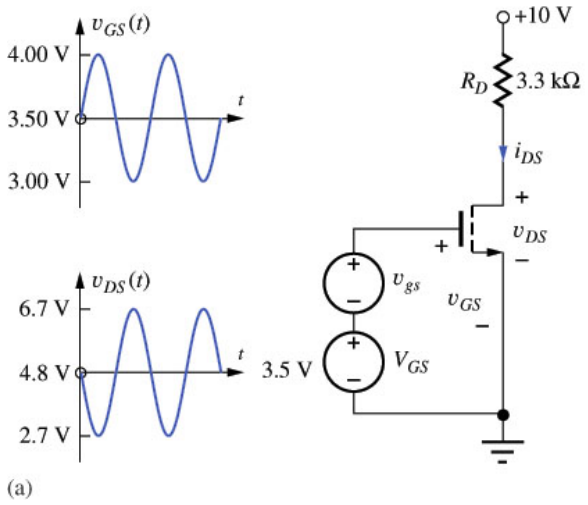
P7.3 J&B Problem 4.56

P7.4 Calculate $v_{CE,SAT}$ for an NPN transistor with $I_C = 1mA$, $I_B = 0.1mA$, $\beta_F = 100$, and $\beta_R = 10$. Use Matlab to plot $v_{CE,SAT}$ and $v_{BE,ON}$ as I_B is swept from $0.1mA$ to $10mA$ with $I_C = 1mA$ and $I_S = 10^{-15}A$.

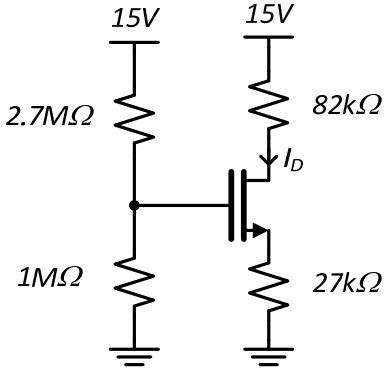
P7.5 Assume the NPN circuit below can be approximated as a linear amplifier. From the plots of $v_{BE}(t)$ and $v_{CE}(t)$ below, what are $v_{be}(t)$, V_{BE}, $v_{ce}(t)$, and V_{CE}? Assume the signals are oscillating at a frequency ω_0.



P7.6 Assume the NFET circuit below can be approximated as a linear amplifier. From the plots of $v_{GS}(t)$ and $v_{DS}(t)$ below, what are $v_{gs}(t)$, V_{GS}, $v_{ds}(t)$, and V_{DS}? Assume the signals are oscillating at a frequency ω_0.



P7.7 Calculate the DC bias current I_D for the circuit on the right assuming $K_n = 250\mu A/V^2$, $V_{tn} = 1V$, and $\lambda = 0$. Calculate the new value of I_D and the percentage change in I_D resulting from a 5% increase in K_n ($K_n = 262.5\mu A/V^2$). Calculate the new value of I_D and the percentage change in I_D resulting from a 5% decrease in V_{tn} ($V_{tn} = 0.95V$).



P7.8 Calculate the DC bias current I_D for the circuit below assuming $K_p = 100\mu A/V^2$, $V_{tp} = -1V$, and $\lambda = 0$. Calculate the new value of I_D and the percentage change in I_D resulting from a 5% increase in K_p ($K_p = 105\mu A/V^2$). Calculate the new value of I_D and the percentage change in I_D resulting from a 5% decrease in V_{tp} ($V_{tp} = -0.95V$).