Prof. Jasprit Singh
Fall 2001
EECS 320

Homework 10

This homework is due on December 6

Problem 1: An n-type $In_{0.53}Ga_{0.47}As$ epitaxial layer doped at 10^{16} cm^{-3} is to be used as a channel in a FET. A decision is to be made whether the JFET or MESFET technology is to be used for the device. In the JFET technology a p^+ region can be made with a doping of 5×10^{17} cm^{-3}. In the MESFET technology a Schottky barrier with a height of 0.4 V is available. Which technology will you use? Give reasons considering gate isolation issues. ($R^* = 5$ Acm$^{-2}K^{-2}$; $D_p = 20$ cm^2/s; $D_n = 50$ cm^2/s; $L_n = 5$ μm; $L_p = 5$ μm.)

Problem 2: Consider an n-channel Si JFET at 300 K with the following parameters:

p^+-doping,	N_a	=	5×10^{18} cm^{-3}
n-doping,	N_d	=	10^{17} cm^{-3}
Channel thickness,	h	=	0.5 μm

(a) Calculate the internal pinch-off for the device. (b) Calculate the gate bias required to make the width of the undepleted channel 0.25 μm.

Problem 3: Consider a GaAs n-channel MESFET at 300 K with the following parameters:

Schottky barrier height,	ϕ_b	=	0.8 V
Electron mobility,	μ_n	=	6000 cm^2/ V $\cdot$ s
Channel width,	Z	=	25 μm
Channel length,	L	=	1.0 μm
Channel depth,	h	=	0.25 μm
Channel doping,	N_d	=	1.0×10^{17} cm^{-3}

(a) Calculate the gate bias $V_{GS} = V_T$ needed for the device to just turn off.
(b) Calculate $V_D(sat)$ for gate biases of $V_{GS} = -1.5$ V and $V_{GS} = -3.0$ V.
(c) Calculate the saturation drain current for the cases considered in part b.

Problem 4: A 500 Å oxide is grown on p-type silicon with $N_a = 5 \times 10^{15}$ cm^{-3}. Assume that the oxide charge is negligible and calculate the surface potential and gate voltage to create inversion at the surface. Calculate the

value of W_{max} for the device. The flat band voltage is -0.9 V.

Problem 5: An Al-gate n-channel MOS capacitor has a doping of $N_a = 10^{16}$ cm^{-3}. The oxide thickness is 500 Å and the flat band voltage is found to be $V_{fb} = -1.0$ V. Calculate the fixed oxide charge.

SOME IMPORTANT ISSUES DISCUSSED THIS WEEK

We have started our examination of the field effect transistors.

FIELD EFFECT TRANSISTORS

The field effect transistors are majority charge devices unlike the BJT. This has advantages in device response since the minority carrier recombination lifetime plays no role in device switching. The technology is also simpler.

The FET technology depends upon controlling the current flowing through a channel by altering the *carrier density* $\times$ *flow area* product. This is done by using a voltage to increase or decrease the band bending in a semiconductor channel.

In the MESFET or JFET technology, the channel charge is produced by doping the semiconductor and the free charge is equal to the doping density. In the depletion region produced by the junction, the mobile charge is essentially equal to zero. Thus by increasing or decreasing the depletion width, the current flowing in the device is changed.

In the MOSFET or MISFET, the channel charge is *induced by band bending by applying a strong bias across an insulator*. This charge is not due to doping and this has many advantages. For example, we don't have to develop a doping technology to create free charge. Also the free carrier density achievable is higher than what we can normally get through doping.

JFETS AND MESFETS

• *Gate Junction*: The gate controls the current flowing in the semiconductor channel by increasing or decreasing the channel depletion region. The gate should have the property that the current flowing in the gate-semiconductor

junction is as small as possible. In principle, we want this current to be zero, but this is not possible.

The gate current depends upon the theory we discussed in the p-n diode (for the JFET) or the Schottky diode (for the MESFET). The JFET current can usually be made very small by a proper choice of the gate doping. The gate should, ofcourse, operate under reverse bias or at low forward bias voltages.

In the case of the MESFET, the gate current is controlled by the Schottky barrier height ϕ_b. If the Schottky barrier is small the MESFET will not work very well and the gate is called a *leaky gate*. Just as we don't want a leaky faucet, we try to avoid a leaky gate.

• *Gate Length*: The gate length controls most of the device performance parameters. It controls the high speed performance of the FET. It also decides how well the gate controls the channel current. The limit on how small the gate length can be made depends upon:

i) The technology available. With optical lithography, it is possible to go down to 0.25 μm. Beyond this one needs electron beam lithography.

• *Channel Design*: The channel doping should be high so that the channel current and its control is maximum. However, at very high doping the channel mobility starts to suffer due to dopant scattering. For high performance MESFETs the channel doping is in the range of 5.0×10^{17} *to* 10^{18} cm^{-3}.

The channel thickness choice depends upon the device application. For high speed devices, the gate length has to be very small, and correspondingly the channel must be very thin as well ($L \sim 2\ h$). If the device is used to drive high current, the channel thickness should be large. however, if the channel is too thick, the gate loses control on the device.

THE MOSFET

We have discussed that in FETs we control the current flowing in a channel by applying a gate bias. In general the current flowing in a channel of area A is

$$I = Ane\mu F$$

where n is the electron density (or hole density for p-type devices). In a MESFET the channel current is controlled by altering the thickness of the region in which electron density is present i.e by changing the value of A. This is done by increasing or decreasing the depletion width by applying a gate bias. The electron density is equal to the doping density. In the MESFET we cannot apply a large forward bias to the gate otherwise there will be a large gate current which is unacceptable.

In a MOSFET we are able to alter the An product by *bending the bands and altering the separation between the conduction bandedge and the Fermi level.* This is possible because in the MOSFET we can apply positive or negative bias on the gate without having to worry about excessive gate current. This is because of the insulator (SiO_2) between the gate and the semiconductor.

By allowing allowing a large band bending it is possible to induce electrons or holes in a MOSFET channel and thus control the current flowing in the device.

The MOSFET is the most important electronic device in modern electronic systems. Its strength comes from the simplicity of its design, reliability of the fabrication process, low cost of the processing steps, and *adequate performance for most applications.* Some issues of importance for a MOSFET are:

• *Oxide-Semiconductor Interface*: In the case of the MOSFET, the electrons (holes) necessary for the current flow are produced by band inversion and not by doping. The carriers move near the oxide (or insulator)-semiconductor interface unlike the MESFET where the carriers move deep in the semiconductor. Thus the quality of the interface is of extreme importance. Due to the very different nature of the crystal structure of Si and SiO_2, it is remarkable that one can get a high quality interface between the two materials.

• *Oxide Quality*: The oxide should be free of impurities which may trap carriers from the channel. It should also have minimum trapped charges which will cause shift in the threshold voltage of the device. The oxide should also be free from any pinhole or other defects which may cause oxide breakdown and a gate breakdown. The thickness of the oxide should be constant under the gate so that the channel charge is produced in a predictable manner.

Important Parameters in the MOS Structure

• *Flat Band Voltage*: The flat band voltage represents the potential difference between the metal and the semiconductor in absence of any applied potential. This is due to the work function difference between the metal and the semiconductor and has a value

$$eV_{fb} = e\phi_m - e\phi_s$$

This is the potential that must be applied to the gate to cause the semiconductor bands to be flat all the way upto the semiconductor-insulator interface.

• *Accumulation, Depletion and Inversion*: By applying a bias on the metal gate, it is possible to bend the semiconductor bands since the insulator prevents any current flow into the gate from the semiconductor or vice versa. If we start with a p-type substrate, the bands can be bent so that near the Si/SiO_2 interface the valence band is closer to the Fermi level than in the bulk region. As a result we have excess holes at the interface. This is the accumulation region.

If the bands are bent so that near the interface the Fermi level is close to the intrinsic Fermi level we have very few mobile carriers at the interface and this is the depletion state.

If we bend the bands so that at the interface there are excess electrons (in a p-type material) we get inversion. A simple criteria used for inversion is

$$V_s = -2\phi_F$$

where V_s is the surface potential in the semiconductor and

$$e\phi_F = E_F - E_{Fi}$$

• *Threshold Voltage*: This is a very important parameter of the MOS device. It represents the gate potential needed to create inversion in the Si channel.

It is important to note that the threshold voltage has a strong dependence on:

(i) Flat band voltage determined by the metal and semiconductor work functions;

(ii) Oxide thickness which must be very carefully controlled;

(iii) Oxide charge which is due to impurities etc. This trapped charge causes a shift in the threshold voltage.

(iv) Doping of the substrate.

TOPICS TO BE COVERED NEXT WEEK

Next week we will finish up our discussion of the MOSFET.

Corrections Please note that on page 379, the right hand side of Eqn 9.4 should not have a negative sign in front. Also Eqn 9.17 on page 383 should not have a + sign between N_a and |.