Homeowrk 11

- The finals for this course are set for Friday December 14, 6:30—
  8:30 pm and Friday Dec. 21, 10:30 am —12:30 pm. Please choose
one of these times and inform me of your choice if you haven’t done
so.
- This homework is not due back to me. However, please do the
homework and check against the solutions that are also given.
- On Dec. 11 we will use the class time to review the various topics
covered in this course.

Problem 1: Problem 9.18 of the text.
Problem 2: Problem 9.20 of the text.
Problem 3: Problem 10.8 of the text.

SOLUTIONS

Problem 9.18  A NMOS with $V_T$ of 1.5 V is operated at $V_{GS} = 5$ V and
$ID_S = 100$ $\mu$A. Determine if the device is in linear or saturation regime.

\[ k = \frac{\mu ZC_{ox}}{L} = 20 \mu A/V^2 \]

Solution

Let us calculate the saturation current for the biasing conditions

\[ I_D(sat) = \frac{k}{2} (V_{GS} - V_T)^2 \]
\[ = 10(3.5)^2 = 122.5 \mu A \]

The current given (100 $\mu$A) is smaller than the saturation current so the device
is in the linear regime. Using the linear expression

\[ ID_S = k(V_{GS} - V_T) V_{DS} \]

we get

\[ V_{DS} = 1.43 \text{ V} \]
Problem 9.20  Threshold bias for an n-channel MOSFET: In the text we used a criterion that the inversion of the MOSFET channel occurs when \( V_s = -2\phi_F \) where \( e\phi_F = (E_F - E_{F_i}) \). Consider another criterion in which we say that inversion occurs when the electron density at the Si/SiO\(_2\) interface becomes \( 10^{16} \text{ cm}^{-3} \). Calculate the gate threshold voltage needed for an MOS device with the following parameters for the two different criteria:

\[
\begin{align*}
d_{ox} &= 500 \text{ Å} \\
\phi_m &= 1.0 \text{ V} \\
N_a &= 10^{13} \text{ cm}^{-3}
\end{align*}
\]

Solution

For the transistor under consideration the value of \( \phi_F \) is given by

\[
\phi_F = -\frac{k_B T}{e} \ln \frac{N_a}{n_i} = -(0.026) \ln \left( \frac{10^{13}}{1.5 \times 10^{10}} \right) = -0.17 \text{ volt}
\]

The surface band bending required for inversion according to the 1\(^{st}\) criterion is

\[
V_s = -2\phi_F = 0.34 \text{ volt}
\]

In the second criteria, the surface bending should be such that the surface electron concentration is \( 10^{16} \text{ cm}^{-3} \). The bulk electron concentration is

\[
n_o = \frac{n_i^2}{p_o} = \frac{2.25 \times 10^{20} \text{ cm}^{-6}}{10^{13} \text{ cm}^{-3}} = 2.25 \times 10^7 \text{ cm}^{-3}
\]

The surface bending needed to generate a surface density of \( 10^{16} \text{ cm}^{-3} \) is

\[
V_s(2) = k_B T \ln \frac{n_{(surface)}}{n_{(bulk)}} = 0.026 \ln \left( \frac{10^{16}}{2.25 \times 10^7} \right) = 0.52 \text{ volt}
\]

Thus, according to the second criteria, the surface bending is considerably greater.

The gate voltage needed for inversion is

\[
V_{GS} = V_{fb} + V_s + \frac{\varepsilon_s F_s}{C_{ox}}
\]

According to the 1\(^{st}\) criterion

\[
V_{GS}(1) = V_{fb} + V_s(1) + \frac{(4\varepsilon_s N_a |\phi_F|)^{1/2}}{C_{ox}}
\]
According to the 2nd criterion,

\[ V_{GS}(2) = V_{f_0} + V_s + \frac{(4\epsilon_s N_a V_s(2))^{1/2}}{C_{ox}} \]

\[ C_{ox} = \frac{\epsilon_{ox}}{d_{ox}} = \frac{3.9 \times 8.84 \times 10^{-14} \text{ F/cm}}{(500 \times 10^{-8} \text{ cm})} = 6.9 \times 10^{-8} \text{ F/cm}^2 \]

The 1st criterion gives

\[ V_{GS}(1) = 1.0 + 0.34 + \frac{(4 \times 1.6 \times 10^{-19} \times 11.9 \times 8.84 \times 10^{-14} \times 0.17)^{1/2}}{(6.9 \times 10^{-8})} \]

\[ V_{GS}(2) = 1.355 \text{ volt} \]

\[ V_{GS}(2) = 1.54 \text{ volt} \]

**Problem 10.8** Consider an n-type 1.0 μm FET made from GaAs and Si. The device cutoff frequency is limited by transit time effects. Using the velocity-field relations for electrons in GaAs and Si, estimate the cutoff frequency for the devices when (a) \( V_D = 0.5 \text{ V} \), i.e., for low-power applications and (b) \( V_D = 10 \text{ V} \), i.e., for high-power applications. Assume that the average field in the channel is \( V_D/L \).

**Solution**

i) The average field in the channel is

\[ \bar{F} = \frac{V_D}{L} = \frac{0.5 \text{ V}}{1.0 \times 10^{-4} \text{ cm}} = 5 \times 10^3 \text{ V/cm} \]

The velocity in GaAs and Si is from Appendix B

\[ v(\text{GaAs}) = 1.5 \times 10^7 \text{ cm/s} \]
\[ v(\text{Si}) = 7 \times 10^6 \text{ cm/s} \]

The transit time for the GaAs device is

\[ t_{tr} = \frac{1.0 \times 10^{-4} \text{ cm}}{1.5 \times 10^7 \text{ cm/s}} = 6.67 \times 10^{-12} \text{ s} \]

The cutoff frequency is

\[ f_T = \frac{1}{2\pi t_{tr}} = 23.86 \text{ GHz} \]

The transit time for the Si device is

\[ t_{tr} = \frac{1.0 \times 10^{-4} \text{ cm}}{7 \times 10^6 \text{ cm/s}} = 1.43 \times 10^{-11} \]
\[ f_T = 11.1 \text{ GHz} \]
ii) The average field is

\[ \bar{F} = \frac{10 \text{ V}}{1.0 \times 10^{-4} \text{ cm}} = 10^5 \text{ V/cm} \]

In this case, the electron velocity in GaAs and Si is about 10^7 cm/s. The cutoff frequency is about 16 GHz in both devices. The example shows the benefits of GaAs and Si over low power applications.
ADVANCED COURSES YOU CAN TAKE IF YOU ARE INTERESTED IN SEMICONDUCTOR DEVICES AND PHYSICS

EECS 421: This course covers more details of semiconductor devices. It is an advanced version of EECS 320.

EECS 423 and 425: These are good courses on semiconductor fabrication issues.

EECS 420: This course would be useful for students who want to have a better understanding of quantum mechanics and its applications in technology.
A TRIAL FINAL EXAM WITH SOLUTIONS

Problem 1: (10 points)

A Si $p-n$ diode is reverse biased at 5.0 V. Electrons from the p-side enter the depletion region and are swept away by the depletion region field to the n-side. Calculate and plot the velocity versus distance as the electrons go from the p-side depletion region edge to the n-side.

$$N_d = N_n = 10^{16} \text{ cm}^{-3}$$

The electron velocity-field relation is

$$v = \frac{\mu F}{1 + \frac{\mu}{v_s}}$$

with $\mu = 1000 \text{ cm}^2/\text{V.s}$ and $v_s = 10^7 \text{ cm/s}$.

In this problem we have to use the discussion in Section 5.2 to obtain the field profile in the depletion region of a diode. The field increases linearly from the p-side depletion region, $-W_p$, to the p-n junction point and then decreases towards zero at the n-side depletion region edge, $W_n$.

On the p-side the depletion region field is

$$F(x) = -\frac{eN_av}{\epsilon} - \frac{eN_aW_p}{\epsilon}$$

We can see that the built in voltage of the diode is 0.7 V. The depletion region width on the p-side and n-side can be calculated to be (total voltage is 5.7 V)

$$W_p = 6.1 \times 10^{-5} \text{ cm} = W_n$$

The maximum field at $x = 0$ is

$$F_m = -\frac{eN_aW_p}{\epsilon} = 9.3 \times 10^4 \text{ V/cm}$$

We see that the velocity values are:

$$x = -W_p = -0.61 \mu\text{m} : F = 0; \quad v = 0$$
$$x = -0.31 \mu\text{m} : F = 4.65 \times 10^4 \text{ V/cm}; \quad v = 7 \times 10^6 \text{ cm/s}$$
$$x = 0 : F = 9.3 \times 10^4 \text{ V/cm}; \quad v = 9.03 \times 10^6 \text{ cm/s}$$
$$\text{etc.}$$

The velocity distance curve is symmetric around $x = 0$. 

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Problem 2: (10 points) In a Si npn BJT a current gain, $\beta$, of 100 is required. Also the transit time of electrons across the base is to be 10 ps.

\[
\begin{align*}
N_{dc} &= 10^{18} \text{ cm}^{-3} \\
N_{de} &= 1.0 \times 10^{16} \text{ cm}^{-3} \\
D_b &= 20.0 \text{ cm}^2/\text{s} \\
L_b &= 15.0 \mu\text{m} \\
D_e &= 10.0 \text{ cm}^2/\text{s} \\
L_e &= 5.0 \mu\text{m}
\end{align*}
\]

Emitter dimensions $= 100\mu\text{m} \times 100\mu\text{m}$

(i) Calculate the base width needed for the device.

(ii) Calculate the base doping needed for this device.

(iii) In 3—4 sentences describe the problems with this device and how these problems can be solved by using a heterojunction bipolar transistor.

You may make the following approximations:

- The device is in the forward active mode and the reverse bias collector current is zero.
- $W_b$ is much smaller than $L_b$.

To find the base width needed we use the relation for the transit time across the base (remember there is no field across the base and the charge flows by diffusion, not drift; see Example 3.17 or Eqn. 7.99)

\[t_{tr} = \frac{W_b^2}{2D_b}\]

This gives for the base width needed

\[W_b = \sqrt{2(20 \text{ cm}^2/\text{s})(20 \times 10^{-12} \text{s})} = 0.2 \mu\text{m}\]

Using the desired value of $\beta = 100$ we now find that the base doping is

\[N_{ab} = N_{io} = 4.85 \times 10^{17} \text{ cm}^{-3}\]

In this device the base is quite thin and the device will therefore suffer from Early voltage problems and punch through problems. In the HBT the base can be doped very heavily and the gain can still be large. Thus we can have a high speed and high gain device.

Problems 3: (10 points)

An n-MESFET is made from GaAs and the maximum acceptable gate current density is $1.0 \mu\text{A/cm}^2$. A power supply is available that can provide a $V_{GS}$ value of $\pm 5.0 \text{ V}$. 

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The device parameters are:

\[
\begin{align*}
& e\phi_b = 0.8 \text{ V} \\
& h = 0.15 \mu\text{m} \\
& N_d = 2 \times 10^{17} \text{ cm}^{-3} \\
& L = 2.0 \mu\text{m} \\
& Z = 20.0 \mu\text{m} \\
& \mu_n = 6000 \text{ cm}^2/\text{V.s} \\
& \epsilon = 13\epsilon_0
\end{align*}
\]

(i) What is the range of \(V_{GS}\) that is allowable for the device.
(ii) Calculate the maximum transconductance, \(g_m\), of the device in the saturation region.

We use the Schottky diode equation to find the prefactor, \(J_s\), of the current that would flow in the gate-semiconductor junction.

\[
J_s = R^* T^2 \exp \left( -\frac{e\phi_b}{k_BT} \right)
\]

Using \(R^* = 8 \ \text{Acm}^{-2}\text{K}^{-2}\) for GaAs we get

\[
J_s = 3.12 \times 10^{-8} \ \text{A/cm}^2
\]

The maximum forward bias that we can have before the gate-semiconductor current density reaches \(1 \mu\text{A/cm}^2\) is then given by

\[
10^{-6} \ \text{A/cm}^2 = 3.12 \times 10^{-8} \ \text{A/cm}^2 \exp(eV/k_BT)
\]

This gives \(V = 0.09\) V. This is the upper limit on the gate bias \(V_{GS}\).

For the device we can see that \(V_{bi} = 0.78\) V and \(V_p = 3.13\) V. The lower limit on the gate bias is then \(V_{GS} = -(3.13 - 0.78) = -2.4\) V.

The transconductance in saturation is given by

\[
g_m(sat) = g_0 \left( 1 - \left( \frac{V_{bi} - V_{GS}}{V_p} \right)^{1/2} \right)
\]

This gives (using \(V_{GS} = 0.09\) V)

\[
g_m(sat) = 1.5 \times 10^{-2} \ \text{S}
\]

**Problem 4:** (10 points)

Consider an n-MOSFET at room temperature. The device is to be used as a load resistor in a circuit and is biased so that \(V_{GS} = V_{DS}\). The resistance of the MOSFET (i.e. \(V_{DS}/I_D\)) is to be 100 k\(\Omega\) when \(V_{DS} = 3.0\) V.
(i) Calculate the width of the gate, \( Z \), needed to accomplish this.

(ii) Note that the MOSFET resistance changes with \( V_{GS} \) or \( V_{DS} \) value.

Calculate the MOSFET resistance at \( V_{DS} = 3.5 \) V.

The other parameters for the device are the following:

\[
\begin{align*}
\mu_n & = 600 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \\
\text{Gate Length} & = 2.0 \mu\text{m} \\
\text{\( d_{ox} \)} & = 500 \text{ Å} \\
V_T & = 1.0 \text{ V}
\end{align*}
\]

In this problem we can see that since we always have \( V_{DS} > (V_{GS} - V_T) \), the device is in saturation. At a bias of \( V_{DS} = 3.0 \) V the current is

\[
I_D = \frac{3.0V}{10^3 \Omega} = 3 \times 10^{-5} \text{ A}
\]

We then have

\[
3 \times 10^{-5} \text{ A} = \frac{Z\mu C_{ox}}{2L}(V_{GS} - V_T)^2
\]

This gives \( (C_{ox} = 6.89 \times 10^{-4} \text{ F/m}^2) \)

\[
Z = 0.72 \mu\text{m}
\]

Using the value of \( Z \) and noting that the device is in saturation we find that at a bias of \( V_{DS} = 3.5 \) V,

\[
I_D = 4.65 \times 10^{-5} \text{ A}
\]

The resistance is then 75.2 kΩ.