

EECS 370

Discussion 10

Week of 4/3 – 4/9

- I)** Project 4: cache simulator
 - a.** Cache properties
 - i.** Write policy: write-back
 - ii.** Associativity: varies (parameter)
 - 1.** Blocks per set given
 - iii.** Size: varies (calculated using other parameters)
 - iv.** Block size: varies (parameter)
 - v.** Replacement policy: LRU
 - b.** Cache accesses through lw, sw, and instruction fetches
 - c.** Info you need for each block
 - i.** Dirty bit
 - ii.** Valid bit
 - iii.** LRU information
 - iv.** Tag
 - d.** Storing to memory (sw)
 - i.** If not in cache, move memory blocks to cache
 - ii.** Then, write to cache
 - iii.** Memory will be updated when that block is evicted
 - e.** Hints
 - i.** Max cache size is 256 blocks, so no need to dynamically allocate memory
 - ii.** Think carefully about how to implement LRU
 - 1.** Counter?
 - iii.** Don't worry about efficiency, you will probably have to iterate through the cache multiple times for each instruction