

# EECS 370 Winter 2009

## Homework 6

**Assigned:** Tuesday, April 7, 2009  
**Due:** Tuesday, April 21, 2009 (in class)

Name: \_\_\_\_\_ Uniqname: \_\_\_\_\_

### Instructions:

1. Please write your name and unickname in the spaces provided above. *Attach this cover sheet* to your completed solutions to the problems listed and turn them in at class on the due date. Submissions without a completed, attached cover sheet cannot be graded.
2. Your answers should be neat, clear, and concise. Computer-written work is recommended (but not required). Show all your work, and state any special or non-obvious assumptions you make.
3. You may discuss your solution methods or your answers with other students, but the solutions you submit must be your own.

### Scores:

<b>Problem #</b>	<b>Points</b>
1	/10
2	/5
3	/10
<b>Total</b>	<b>/25</b>

**Problem 1** (10 points)

Suppose you are given a system with the following specifications:

- 32-bit virtual address space
- 1GB of physical memory
- 2KB pages
- 4B page entries

Design a hierarchical virtual memory framework.

a) (2 points) How many virtual pages are there?

b) (2 points) How many physical pages?

c) (3 points) Assume each page table must fit in a single page. How many levels of page tables are required? How many entries are in each table?

d) (3 points) Assume your virtual memory system is optimally designed. (HINT: how many bits should your superpage number represent? Do you want this number to be high or low?) What is the worst-case page table size of this hierarchical configuration? What are the advantages of this hierarchical design over a "flat" design? What are the disadvantages?

**Problem 2: Cache Addressing** (5 points)

A high-performance computer has a cache with the following characteristics:

- 50-bit addresses
- byte-addressable memory
- 16 megabyte cache size (1 megabyte =  $2^{20}$  bytes = 1,048,576 bytes)
- 2 kilobyte cache block size (1 kilobyte =  $2^{10}$  bytes = 1,024 bytes)
- 16-way set-associative cache

Address bit numbering: most significant bit is bit 49, least significant bit is bit 0.

a) What range of address bit numbers are used for each of the following?

<u>Field</u>	<u>Number of Bits</u>	<u>Bit Range</u>
<b>Tag</b>		
<b>Set Index</b>		
<b>Block Offset</b>		

b) For address **0x 3 2354 BA38 BE0F**, show the tag, set index, and block offset. You may state your answers in either binary or hexadecimal format.

<u>Field</u>	<u>Binary / Hexadecimal</u>
<b>Tag</b>	
<b>Set Index</b>	
<b>Block Offset</b>	

**Problem 3** (10 points)

Consider the following computer with a CPU, data cache, and memory.

- The system has a 12-bit virtual address size, and the size of a virtual memory page is 256 bytes. The computer has 65536 bytes of physical memory.
- The size of the CPU data cache is 512 bytes, with a block size of 16 bytes. The CPU data cache is 2-way set-associative with LRU replacement, and it is a virtually indexed cache. For a hit, the data cache can be accessed in a single clock cycle. For a miss, a cache block in memory can be read in 10 clock cycles, which includes the time for a TLB access.
- The CPU includes a fully associative TLB with 2 entries and an LRU replacement policy. For a TLB miss, the appropriate page table entry is supplied to the CPU after 25 clock cycles. The system uses a single level page table. Assume the TLB and the data cache are initially empty. The contents of the page table are shown below:

VPN	Valid	PPN
0	0	-
1	1	0xfd
2	1	0x4b
3	0	-
4	1	0x55
5	1	0x32
6	1	0x54
7	0	-
8	0	-
9	1	0xfe
A	1	0xfc
B	0	-
C	1	0xba
D	1	0x01
E	0	-
F	0	-

a) (7 points) Data reads from the following virtual addresses are performed (in the order listed):

0xce2, 0x258, 0xcea, 0x2d4, 0x15b, 0x241, 0xcee.

Please complete the table below to show the following for each read:

- Physical address (show it in hex)
- Data cache hit/miss (write HIT or MISS as appropriate)
- TLB hit/miss (write HIT or MISS as appropriate, or write NA if the TLB is not accessed)

Virtual Address	Physical address	Data cache hit/miss	TLB hit/miss/NA
0xce2			
0x258			
0xcea			
0x2d4			
0x15b			
0x241			
0xcee			

b) (3 points) A program running on the above described computer has a data cache miss rate of 15% and a data TLB miss rate of 10%. What is the average memory access latency for this program for data accesses? Please show your work and clearly state any assumptions you make.